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Assessing the potential of TOPCon solar cells architecture using industrial n-type cast-mono silicon material

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Abstract. Cast-mono silicon material is interesting for its lower carbon footprint compared to Czochralski (Cz) monocrystalline silicon. However, solar cells fabricated using cast-mono (CM) silicon show lower performances. In this work, two routes to make cast-mono silicon advantageous over Cz silicon are considered. The first route is to further reduce carbon footprint of cast-mono silicon, by using Upgraded Metallurgical Grade silicon (UMG-Si) feedstock instead of Solar Grade silicon (SoG-Si) feedstock. TOPCon solar cells are fabricated using both feedstocks, and cast-mono growth technology, using industrial-type furnaces. Laboratory studies show that UMG-Si can result in efficiencies higher than solar cells made of SoG-Si when feeding the material to a CM crystallization process. But when compared to Cz, CM-UMG-Si TOPCon solar cells conversion efficiency values are still $0.5\%_{abs}$ lower. The second route is to take advantage of the TOPCon passivation layer (e.g., poly-Si) ability to getter metallic impurities, and thus improve the quality of cast-mono material. Several TOPCon sequences are tested and their effect on the carrier recombination properties of the device are studied. In the end, solar cells are fabricated and again, UMG-Si solar cells show better results than SoG-Si solar cells, with efficiency up to 22.65%, independently confirmed.

Keywords: Cast-mono / SoG / UMG / TOPCon

1 Introduction

Cast-mono silicon (CM-Si) is a hybrid material between Czochralski monocrystalline silicon (Cz-Si) and cast grown multicrystalline silicon [1]. During the ingot crystallization, the seeds deposited at the bottom of the crucible allow a controlled growth with the same crystal orientation as the seeds, usually <100>. Compared to Cz material, cast-mono wafers contain more metallic impurities mainly originating from the crucible and crystal defects such as dislocations appearing during the growth. Such drawbacks lead to lower overall performances of the cast-mono material. This reduced performance is counterbalanced by lower production costs and lower emissions of greenhouse gases [2].

The replacement of Solar Grade silicon (SoG-Si) by Upgraded Metallurgical Grade silicon (UMG-Si) is a solution to further reduce the carbon footprint, and production costs [3]. However, as UMG-Si shows higher impurity content (both metallic and non-metallic), the resulting efficiency might be lower than using conventional SoG-Si, purified via Siemens process. In order to enhance performances of UMG-Si, a gettering step can be implemented to remove metallic impurities prior to solar cell processing [4,5].

Industrial TOPCon sequences have been used successfully on n-type cast-mono Si wafers [6]. This study aims to compare the use of these two SoG-Si and UMG-Si materials, using n-type silicon wafers produced in an industrial-size furnace. To evaluate the potential of each cast-mono material, TOPCon solar cells are fabricated, as it is state-of-the-art architecture, and it shows high gettering potential [7,8].

It was shown previously that the gettering effectiveness can be enhanced by optimizing TOPCon sequence, using less stoichiometric oxide or with higher amount of pinholes [9], or higher diffusion/anneal temperature [10] for example. The second part of this work aims to test several TOPCon sequences, as the gettering potential differs, depending on the type of process used.

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Table 1. IV parameters of the TOPCon solar cells fabricated from different material types (Cz-Si, CM-UMG and CM-SoG). The results are averaged out of 6–9 cells with optimized firing temperature. These measurements are in-house measurements, the front contact is obtained by GridTouch, the rear contact by a non-conductive dark chuck together with rear contacting pins.

Si material	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	η (%)	pFF-FF (%)	FF_0-pFF (%)
Cz-Si	695.8	40.28	80.1	22.45	3.4	1.1
CM-UMG	689.8	40.14	79.2	21.94	3.2	2.1
CM- SoG	684.5	40.22	77.7	21.40	3.7	3.0

2 Experimental details

The wafers used in this study originate from two 650 kg industrial size Phosphorus-doped ingots, grown either using SoG-Si feedstock or using UMG-Si feedstock. SoG-Si is purified via Siemens process [11]. UMG-Si is obtained from metallurgical silicon, after adding several purification steps. UMG-Si is a compensated silicon, as it contains both polarity type dopants (donors and acceptors). Additional details about the process, the purity of silicon and the amount of impurities are available in literature [4,12].

15.7 cm × 15.7 cm n-type cast-mono Si wafers produced from these ingots show resistivities of 1.6–1.9 Ω.cm and 0.6–0.9 Ω.cm for cast-mono SoG-Si (CM-SoG) and cast-mono UMG-Si (CM-UMG) respectively. N-type Cz wafers, with resistivity of 0.9–1.1 Ω.cm are added as references. Cz-Si originates from SoG-Si purified via Siemens process.

CM-Si crystallization results in the formation of dislocations clusters originating from different crystal defects [13–15]. The dislocation generation is hardly controllable, and the amount and the distribution of the dislocations differ from one ingot to another. Thus, the variation of the dislocation rate is more a crystal growth issue than a feedstock type effect. In the present study, for each ingot (CM-SoG and CM-UMG), wafers are coming from 2 different bricks. In each brick, the dislocation growth varies so the position and rate of dislocation within the wafer are different. Bricks 1 and 2 are associated to the UMG-Si ingot and Bricks 3 and 4 are linked to SoG-Si ingot.

TOPCon solar cells fabrication first consists in saw damage removal followed by random pyramid formation in alkaline solution. A tube furnace diffusion using BBr_3 forms a 150 Ω/sq boron emitter. The unwanted emitter is removed by single side Borosilicate Glass (BSG) etch followed by alkaline silicon removal in a batch system and the unwanted emitter and borosilicate glass on the rear side are removed. In the standard process, the TOPCon stack consists in a thermally grown tunnel oxide and an in situ doped polysilicon layer, both formed subsequently in a low-pressure chemical vapor deposition tube. The parasitic deposition on the front side is then chemically removed and followed by annealing and both sided surface passivation (ALD-Al_2O_3 + SiN_x:H). Finally, screen-printing is applied, using Ag-Al paste on front side and Ag paste on the back side followed by contact firing in a conventional belt furnace. The laser-enhanced contact optimization (LECO) step is applied at the end of the process [16]. The metallization and firing processes used in this study are compatible with the LECO process. This process is called in the following standard process. Additional TOPCon sequences will be applied and described in the results sections.

Symmetrical lifetime samples are also fabricated. In order to take into account all the high temperature process steps, the samples first underwent the boron diffusion (after texturing and cleaning). After boron diffusion, the $p+$ layer is removed and the TOPCon sequence is applied on both sides to all samples, varying several parameters (tunnel oxide type, doping process, poly-Si thickness and anneal temperature). Finally, the samples are passivated and fired. Quasi-steady-state photoconductance (QSSPC) measurements determine the $iV_{oc,max}$ which corresponds to the maximum implied V_{oc} achievable, as the boron diffused layer is removed beforehand. Due to some non-linearities of the fit of the inverse lifetime curve the extraction of reliable J_{0e} and τ_{bulk} for the full data set was not possible. The best comparable data are therefore the $iV_{oc,max}$. The electrical properties of the cells are characterized by current voltage (IV) measurements in light illumination at 25 °C (AM1.5 global spectrum). Photoluminescence imaging are carried out on the cells.

3 Comparison of solar cells results from cast-mono and Cz wafers

3.1 Solar cell results

The first part of this study aims to compare solar cells fabricated from Cz-Si and CM-Si wafers, obtained with two silicon feedstocks: SoG-Si and UMG-Si. Standard process is used for the TOPCon sequence for the solar cells, as described in part 2. The average efficiency difference is $0.51\%_{abs}$ between Cz-Si and the best CM-Si efficiencies, while the maximum efficiencies are 22.52% and 22.25% for Cz-Si and CM-UMG, respectively. The efficiency gain for Cz-Si is due to an increase of all IV parameters. Contrary to Cz-Si, CM-Si contains, for both UMG-Si and SoG-Si, dislocation clusters and metallic impurities lowering bulk lifetime and affecting the solar cells parameters [6,17].

Table 1 shows the solar cells results obtained for the 3 types of wafers i.e. Cz-Si, CM-SoG and CM-UMG. The average efficiency difference is $0.51\%_{abs}$ between Cz-Si and the best CM-Si efficiencies, while the maximum efficiencies are 22.52% and 22.25% for Cz-Si and CM-UMG, respectively. The efficiency gain for Cz-Si is due to an

increase of all IV parameters. Contrary to Cz-Si, CM-Si contains, for both UMG-Si and SoG-Si, dislocation clusters and metallic impurities lowering bulk lifetime and affecting the solar cells parameters [6,17].

Comparing CM-UMG to CM-SoG, the efficiency of CM-UMG is $0.54\%_{abs}$ higher than the efficiency of CM-SoG caused by an increase of V_{oc} and *FF*.

To assess the *FF* losses, three parameters are considered. The Fill Factor (*FF*) is extracted from the illuminated IV curve. The pseudo–Fill Factor *(pFF)*, which is free from resistive losses, is extracted from the Suns-Voc curve. The ideal Fill Factor (FF_0) which is free from resistive losses, shunt and space charge region (SCR) recombination losses, is calculated from the ideal IV curve [18,19]. Consequently, as shown in [20], *pFF-FF* stands for *FF* losses due to series resistance while FF_0-*pFF* shows *FF* losses due to SCR recombination, as long as the parallel resistance exceeds 4500 $\Omega.cm^2$; which is the case in the following.

The loss in *FF* for the CM-SoG cells is firstly due to higher series resistance, resulting in higher *pFF-FF* for CM-SoG compared to CM-UMG as the resistivity of CM-SoG is higher than for CM-UMG. Furthermore, UMG-Si contains more metallic impurities than SoG-Si, resulting in the creation of recombination centers within the SCR. Consequently, FF_0-*pFF* for CM-UMG should be higher than FF_0-*pFF* for CM-SoG. The contrary is observed in Table 1: FF_0-*pFF* for CM-UMG is lower than for CM-SoG; meaning that the recombination losses within the SCR are lower for CM-UMG than for CM-SoG.

The effect of resistivity is first addressed to understand the results obtained for CM-SoG. Indeed the higher resistivity of CM-SoG leads to higher SCR width [21], and in this case, recombination within the SCR are higher [21,22], explaining the higher FF_0-*pFF* for CM-SoG.

Moreover, the spatial repartition of the dislocation within the wafers has to be considered, as dislocations create additional shunt paths within the space charge region [23]. Figure 1 shows PL images of cells for the three studied materials. For CM-SoG and CM-UMG, two PL images are shown, corresponding to the 4 different groups of cells described in the experimental part, with different dislocations locations and concentrations, representative of the other cells. Unfortunately, quantitative values of the dislocation rate are not available for the wafers in the present study. The comparison is thus qualitative, considering the PL images shown in Figure 1.

Figure 1 also shows that when the dislocation rate is very low, as for Brick 1, V_{oc} and FF_0-*PFF* are close to Cz results. As the dislocation rate increases, as for Brick 4, FF_0-*PFF* increases and V_{oc} decreases. It turns out that the wafers from SoG material (Bricks 3 and 4) have a highest amount of dislocations, resulting in higher losses both for V_{oc} and *FF*. As mentioned in Section 2, this is rather due to the crystal growth itself than to the effect of the feedstock type.

3.2 Symmetrical lifetime samples results

In order to confirm the detrimental influence of the dislocation, $iV_{oc,max}$ measurements on symmetrical samples passivated with TOPCon layers were conducted either on dislocation free parts of the sample and dislocated regions of the samples using QSSPC setup. Standard process is used for the TOPCon sequence for all samples. The results are shown in Table 2.

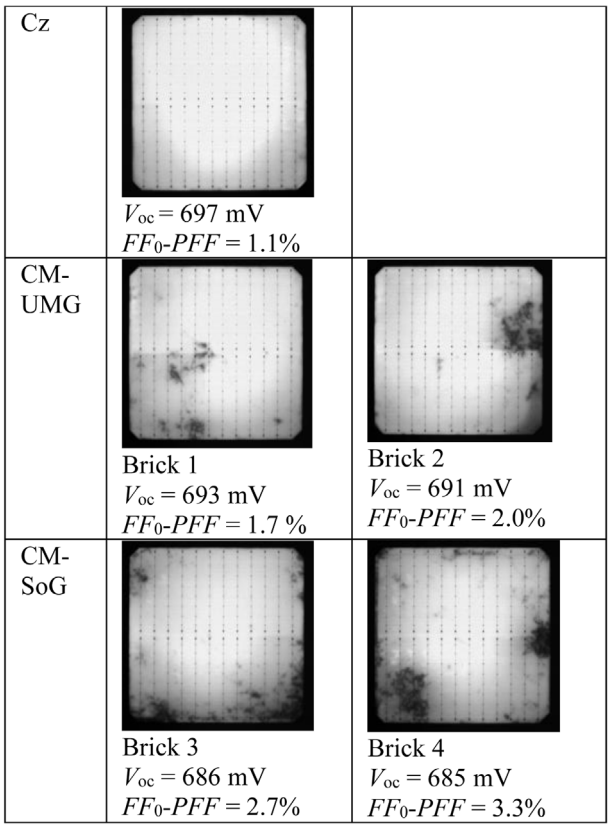

Fig. 1. PL images of representative cells, for three materials, Cz, CM-SoG and CM-UMG. For each cell, the corresponding V_{oc} and FF_0-*PFF* values are depicted.

On regions containing dislocations, $iV_{oc,max}$ is lower compared to dislocation free regions, confirming the detrimental influence of dislocations on V_{oc}. Moreover, $iV_{oc,max}$ for CM-SoG is lower than for CM-UMG, as the dislocation clusters are denser for CM-SoG, as shown in Figure 1.

On dislocation free regions, $iV_{oc,max}$ for CM-UMG and CM-SOG are closer to Cz values. The difference between Cz and CM-Si is partly due to the metallic impurities, which might be removed using efficient gettering. Note that $iV_{oc,max}$ is slightly higher for CM-UMG than for CM-SoG, most probably because CM-UMG resistivity is lower.

4 Optimization of the TOPCon process

As shown in the previous section, there is a gap between the Cz and CM efficiencies, explained by the presence of dislocations and metallic impurities. However, the TOPCon layer generates a strong impurity gettering effect, removing metallic impurities such as iron [24]. Even though the authors conducted their experiment on *p*-type substrate, one can assume that a positive effect of enhanced gettering should be reached on *n*-type substrate, as *n*-type material also well reacts to phosphorus gettering [17,25].

Table 2. $iV_{oc,max}$ measurements obtained from QSSPC measurement conducted on both dislocation free and dislocated region for three materials, Cz, CM-UMG and CM-SoG. The results are averaged out of 4–6 wafers.

	$iV_{oc,max}$ in dislocation free region (mV)	$iV_{oc,max}$ in dislocated region (mV)
Cz	710	NA
CM-UMG	704	694
CM-SoG	703	678

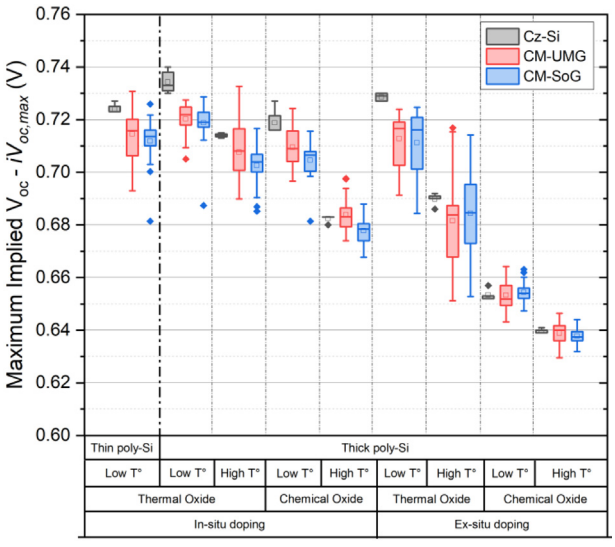

Fig. 2. Variation of the $iV_{oc,max}$ as a function of the material type and on the recipe parameters: thin or thick poly-Si, in situ or ex situ doping, thermal or chemical oxide and high or low temperature. The values shown are mean values of 4–8 samples.

The second part of this work thus deals with the optimization of the TOPCon process to enhance the impurity gettering. In order to test the ability of the TOPCon layer to getter, several TOPCon process steps are modified: the type of tunnel oxide (chemical or thermal), the doping process (in situ or ex situ, using $POCl_3$ diffusion), the poly-Si layer thickness (low – 80 nm or high – 150 nm) and the anneal temperature (low – 900 °C or high – 950 °C). The ramping down rate during the anneal step is kept similar for both temperatures.

4.1 Symmetrical lifetime samples results

The experiment deals with the evaluation of $iV_{oc,max}$ for the different TOPCon sequences, as described above. Figure 2 shows the variation of the $iV_{oc,max}$, for the three types of material, i.e. Cz-Si, CM-UMG and CM-SoG and for all the TOPCon processes tested. The standard sequence corresponding to a thermal oxide with a thin poly-Si, an in situ doping and a low temperature thermal annealing, is shown on the left-hand side of the graph (Thin poly-Si).

In order to take into account, the different spatial positions of the dislocations within the sample (as discussed in the previous section), the measurement are done in 5 different positions (center and 4 corners) which explain the highest dispersion of $iV_{oc,max}$ for CM-Si. Thus apart from the dispersion due to the dislocations, average $iV_{oc,max}$ of CM-UMG and CM-SoG remain similar whatever the TOPCon process.

Overall, the CM-Si $iV_{oc,max}$ results follow the same trend as Cz-Si results. Even though some parameters such as chemical oxide, high temperature or thicker poly-Si have more potential for enabling external gettering, $iV_{oc,max}$ is dominated by the surface passivation quality.

Below is a detailed analysis on the effect of process steps on the surface passivation quality.

Higher anneal temperature – Using a higher annealing temperature always leads to a degradation of $iV_{oc,max}$. Indeed the increase in temperature leads to a stronger in-diffusion of the dopants within the bulk Si. This in-diffused region adds Auger and Shockley Read Hall (SRH) recombination, which is not compensated by the better field effect passivation of the poly-Si and the in-diffused region [26].

Chemical oxide – As demonstrated earlier [27,28], the chemical oxide is less dense and off-stoichiometric compared to thermal oxide, resulting in a decreased passivation quality. Moreover, chemical oxide is more sensitive to higher temperature annealing, leading to an additional loss in $iV_{oc,max}$. The stronger thermal expansion of the tunnel oxide induces stress within the layer and damages the tunnel oxide, lowering the chemical surface passivation and facilitating the phosphorus atoms in-diffusion (leading to higher Auger and SRH recombination).

Ex situ doping – The ex situ doping is more detrimental, especially for chemical oxide and higher temperature. No dopant profiles are available. However, even though the maximum temperature is the same for in situ and ex situ doping, the dopant profile should differ as the diffusion sequence is different. One can hypothesize that the in-diffusion beyond the tunnel oxide is more pronounced for ex situ doping.

Thicker poly-Si – Using a thicker poly-Si layer leads to an increase of the $iV_{oc,max}$ up to 740 mV for Cz-Si and 727 mV for UMG-Si. This is due to the increased electric field of the thicker poly-Si layer. Moreover, the process modification induced using a thicker poly-Si layer results in a slightly different dopant profile, leading to a higher passivation quality.

4.2 Solar cell results

Following the lifetime samples measurements, solar cells are fabricated using the two optimum TOPCon sequences in addition to the standard process used in Section 3. The results for the standard process are the same as the ones presented in Table 1. While ex situ doping at low

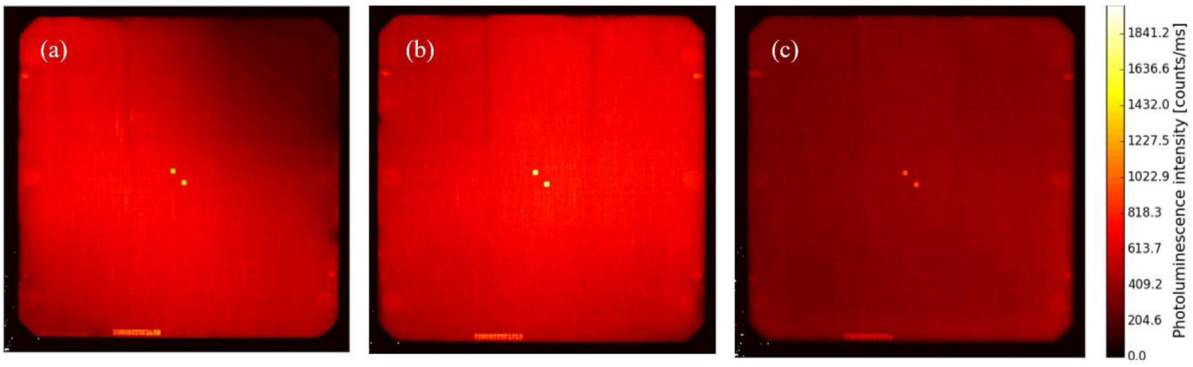

Fig. 3. PL image of the symetrically passivated Cz-Si samples for (a) ex situ doping at low temperature with thermal oxide (b) in situ doping at low temperature with thermal oxide and (c) in situ doping at low temperature with chemical oxide.

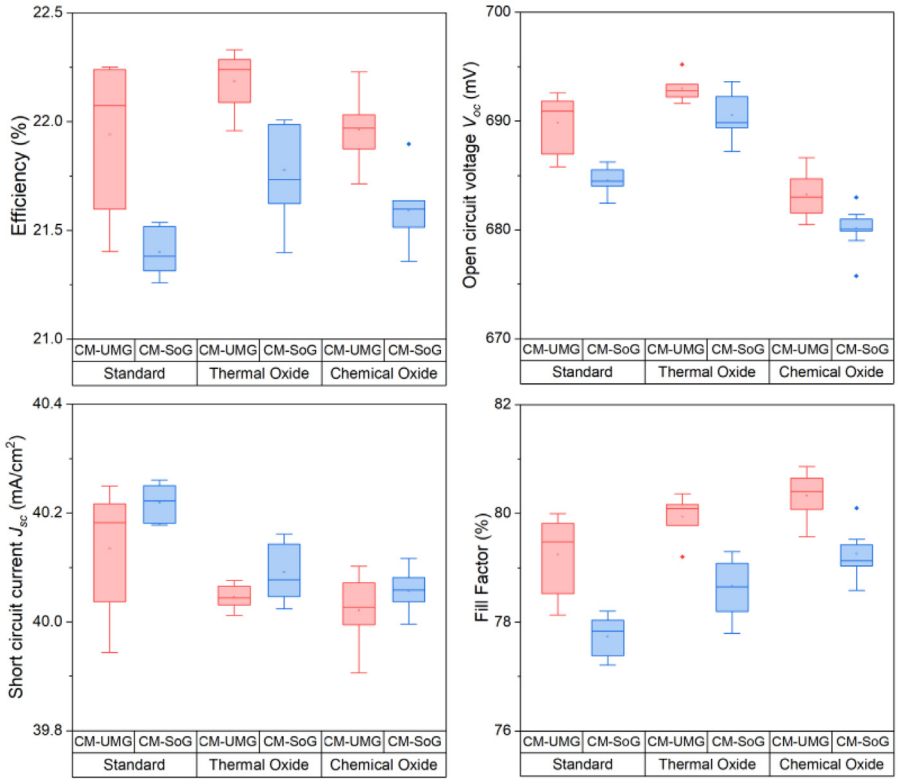

Fig. 4. Solar cells I/V results (a) efficiency (b) V_{oc} (c) J_{sc} and (d) *FF* as a function of the TopCon sequence, for CM-UMG and SoG-UMG. The results are averaged out of 6–9 cells with optimized firing temperature.

temperature with thermal oxide gave good $iV_{oc,max}$ results, lifetime inhomogeneities was observed on PL image (Fig. 3a, arrow), which was not the case using in situ doping, for both thermal and chemical oxide (Figs. 3b and 3c, respectively). The solar cell fabrication thus focuses on the best results obtained for in situ doping, defined as:

- Standard: Thermal Oxide + Thin poly-Si + In situ Doping + Low Temperature annealing
- Thermal Oxide: Thermal Oxide + Thick poly-Si + In situ Doping + Low Temperature annealing
- Chemical Oxide: Chemical Oxide + Thick poly-Si + In situ Doping + Low Temperature annealing.

Figures 4a–4d show the solar cells I/V results for the three selected recipes and the two CM-Si materials. Table 3 gives details about the *FF* losses, showing *pFF-FF* and *FF0-PFF* values for the three TOPCon recipes and the two CM-Si materials.

Similarly to the lifetime samples, the efficiency is higher using a thermal oxide associated with a thicker poly-Si layer, compared to the Standard process. The highest efficiency results from an enhancement of V_{oc} (as already observed in previous section) and *FF*. Table 3 shows that thicker poly-Si leads to reduce the series resistance (lower *pFF-FF*) thanks to the higher conductivity of the thicker

Table 3. *FF* losses, i.e. *pFF-FF* and FF_0-*pFF* as a function of the TOPCon recipe, for CM-UMG and SoG-UMG.

	TopCon process	*pFF-FF* (%)	FF_0-*pFF* (%)
CM-SoG	Standard	3.7	3.0
	Thermal	3.5	2.4
	Chemical	2.9	2.1
CM-UMG	Standard	3.2	2.1
	Thermal	2.7	2.0
	Chemical	2.5	1.6

poly-Si layer and/or the lower contact resistance between Ag paste and poly-Si. The lower FF_0-*PFF* shows that the thicker TOPCon layer also reduces the recombination within the SCR. It was shown previously that a thicker layer results in less damage of the oxide layer during fire-through screen-printing contacts consequently mitigating recombination at the metal contacts [29]. There could be also an effect of an enhanced gettering of impurities, thanks to thicker layer, but the two effects cannot be decoupled for now.

Using chemical oxide instead of thermal oxide gives lower efficiency, mainly due to reduced V_{oc} even though *FF* increases. The reduction of V_{oc} is explained by the reduced passivation quality of the TOPCon layer using chemical oxide, as already stated in the previous section. The *FF* increase is both due to a reduction of FF_0-*PFF* and *pFF-FF* (Tab. 3). Using chemical oxide results in the formation of pinholes which facilitate the conduction [30]. The presence of pinholes enables faster gettering [5], leading to a further reduction of the SCR recombination resulting in lower FF_0-*PFF* than thermal oxide.

For both thermal and chemical Oxide, the thicker poly-Si layer leads to lower J_{sc}, due to a higher free carrier absorption of the thicker poly-Si layer [31].

The trend observed in Figure 4 is the same as in Table 1: CM-UMG shows better results than CM-SoG due to the impact of dislocations on both V_{oc} and *FF*.

Finally, the two champion cells using CM-Si and including a thicker poly-Si layer with a Thermal Oxide (Thermal Oxide in Fig. 4) where independently measured at Fraunhofer ISE CalLab in Germany, and result in efficiencies of 22.45% and 22.65% for CM-SoG and CM-UMG respectively (CalLab measurement condition: 12 front bus bars contact on the front side and rear reflective conducting chuck, AM1.5, 1000W/m^2).

5 Conclusion

This study showed that using UMG-Si as feedstock for fabricating cast-mono TOPCon solar cells is a promising option, as the efficiency is only 0.5 $\%_{abs}$ lower than Cz-Si. The harmful effect of dislocation rate has been shown qualitatively, and is especially detrimental for the *FF*, as dislocations create recombination paths within the space charge region. This explains the weaker results obtained with SoG-Si, as the dislocation rate is slightly higher.

Optimizing the TOPCon sequences leads to an additional efficiency gain of +0.4 $\%_{abs}$, using a thicker poly-Si layer coupled with thermal oxide. This enhancement is induced by the increase in V_{oc} and *FF*, thanks to a better surface passivation, a reduced metal recombination and probably to a more effective gettering. For chemical oxide, the better gettering induced by the presence of pinholes does not counterbalance the degradation of the surface passivation, due to the detrimental effect of the pinholes, leading to a decrease of the efficiency.

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Conflicts of interest

No conflicts of interest to declare.

Data availability statement

The data are not publicly available due to privacy or ethical restriction.

Author contribution statement

Conceptualization, B. Bazer-Bachi, J. Posada and P. Saint-Cast; Experimental Work, Characterization P. Saint-Cast and C. Tessmann; Methodology, B. Bazer-Bachi, J. Posada and P. Saint Cast; Formal Analysis, B. Bazer-Bachi, C. Tessmann and P. Saint-Cast; Writing – Original Draft Preparation, B. Bazer-Bachi; Writing – Review & Editing, B. Bazer-Bachi P. Saint-Cast, R. Bodeux, S. Mack; Visualization, J. Posada; Supervision, G. Goaer, S. Mack; Validation, G. Goaer; Project Administration, J. Posada, P. Saint-Cast, B. Bazer-Bachi.

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