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Review

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Wet chemical poly-Si(n) wrap-around removal for TOPCon solar cells

Katrin Krieg[1,*], Sebastian Mack[1], Jan Vollmer[2], Tobias Dannenberg[2], Damian Brunner[2], and Martin Zimmer[1]

[1] Fraunhofer Institute for Solar Energy Systems, Heidenhofstr. 2, 79110 Freiburg, Germany
[2] RENA Technologies GmbH, Höhenweg 1, 78148 Gütenbach, Germany

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Abstract. This work gives an overview on different technological solutions for polysilicon removal in industrial tunnel oxide passivated contact (i-TOPCon) *n*-type silicon solar cell fabrication. The removal of parasitically deposited poly-Si layers on the front and the edges is a mandatory requirement for a low reverse bias junction leakage current (I_{rev}). A polysilicon removal study on wafer level shows (i) that the efficient removal of the surface oxide layer before poly-Si etching is crucial to achieve short etching times and (ii) that an additive in the KOH solution enhances etching selectivity between poly-Si and silicon oxide surfaces. To evaluate the impact on device level, TOPCon cells have been fabricated in parallel using in-situ n-doped PECVD and LPCVD layers, as well as ex-situ LPCVD poly-Si layers, with another variation of poly-Si removal processes, namely wet chemical inline, wet chemical batch cluster and atmospheric dry etching (ADE). Our results show that a two-minute inline polysilicon removal in hot KOH meets the I_{rev} qualification in case of as deposited in-situ doped layers, whereas for ex-situ doped layers a batch process with a five-minute KOH etching time is needed. LPCVD poly-Si cells show efficiencies above 23%, PECVD poly-Si cells with a batch cluster poly-Si removal process up to 23.4%.

Keywords: Ex-situ / in-situ / batch cluster etching / inline etching / wet chemical

1 Introduction

Industrial tunnel oxide passivated contact (i-TOPCon) solar cells are in focus of photovoltaics (PV) industry and research. The deposition of the poly-Si layer on the rear side is a key aspect for TOPCon solar cells. The TOPCon layer stack (tunnel oxide and doped poly-Si) that is needed for carrier selectivity is usually deposited by low pressure chemical vapor deposition (LPCVD), or plasma enhanced chemical vapor deposition (PECVD) [1]. LPCVD n-doped poly-Si layers are currently still mainstream in industry, typically combined with ex-situ doping, i.e. *n*-type doping of an intrinsic Si layer in a following $POCl_3$ diffusion process. The ITRPV 2022 roadmap suggests that transition from LPCVD to PECVD poly-Si deposition will take place in the upcoming years [2]. The doping of the PECVD TOPCon layers is usually done in-situ, i.e. during deposition, because for this technology the deposition rate for in-situ doping is as high as for intrinsic poly-Si. At Fraunhofer ISE, the industrial route of TOPCon technology was based on in-situ phosphorus doped LPCVD layers [3]. All the deposition processes, either LPCVD with loading one wafer per slot or alternatively front-to-front loading or PECVD with a target single side deposition, lead to some wrap-around and therefore a parasitical poly-Si deposition on the front side and the edges [1,4]. For LPVCD the wrap-around to the front side of the solar cell is complete (one wafer per slot), for PECVD only at the edges (Fig.1).

For solar cells, a high-quality edge isolation, i.e. the separation of p and n regions, needs to be ensured. A parasitically deposited n doped poly-Si on the front side and on the wafer edges leads to a low shunt resistance due to direct the contact to the p^+ emitter (Fig. 2). The removal of the poly-Si from the front side and of the edges is thus of utmost importance [1,5]. There are ideas to avoid the wrap-around completely by using physical vapor deposition (PVD) [6] or PECVD masks [7] and this would naturally reduce the required amount of TOPCon process steps [8]. The parasitical poly-Si can successfully be removed by e.g. atmospheric dry etching (ADE, $I_{rev} = 0.12$ A) [9], wet chemical processes using inline HF/HNO_3 and batch KOH ($I_{rev} = 0.15$ A) [5] or wet chemical inline processes using 15 wt.% KOH at 65 °C (parallel resistance $R_p = 31$ kOhm cm^2) [1].

* e-mail: katrin.krieg@ise.fraunhofer.de

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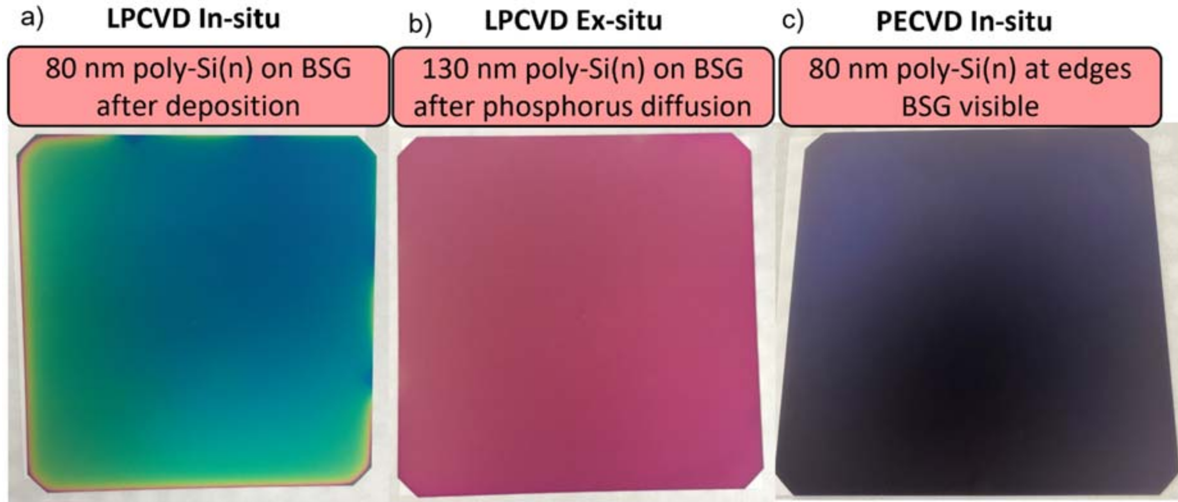

Fig. 1. Poly-Si on borosilicate glass (BSG) on the textured front side for (a) in-situ doped LPCVD poly-Si after deposition, (b) ex-situ doped LPCVD poly-Si after phosphorous doping and (c) in-situ doped PECVD (only BSG visible).

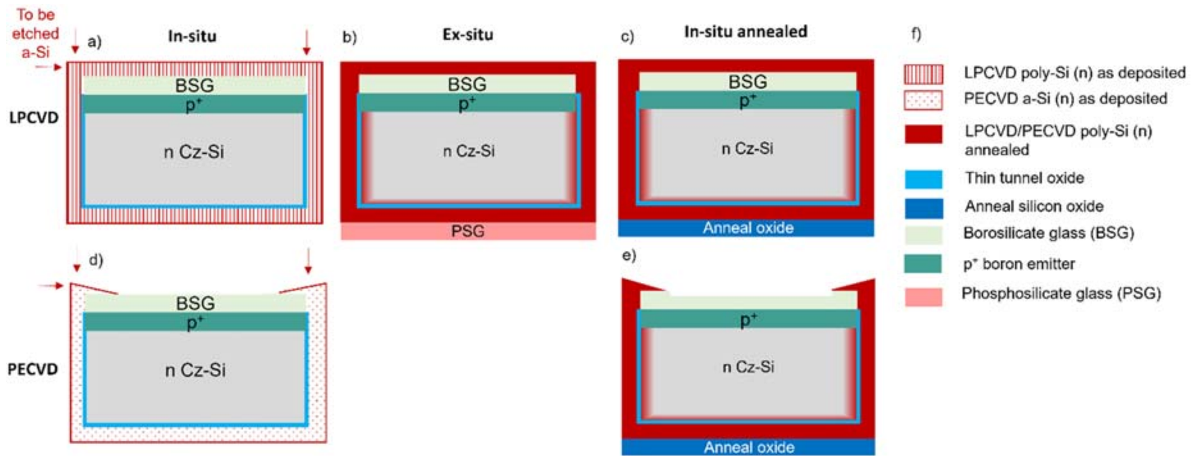

Fig. 2. Cell scheme just before the poly-Si etching process on the textured front side for single slot (a) in-situ, (b) ex-situ and (c) in-situ with anneal oxide route. For (b, c, e) the oxide/glass layer on front and edges was already removed in a single side HF (f) legend.

In this article we focus on wet chemical removal of the parasitical poly-Si in hot diluted potassium hydroxide (KOH) because it is highly relevant for industrial TOPCon cells for reasons of cost efficiency and availability of chemicals in existing production lines. Single side wet chemical etching using KOH has been established successfully to remove the parasitic boron emitter (chemical etch isolation, CEI) on the rear side of TOPCon solar cells [10]. This knowledge can be transferred to poly-Si removal. In general, the single side wet chemical polysilicon removal can be realized as an inline process or as a batch cluster process. An inline process is a roller based single side etching process with direct contact of the wafers to the transport rollers. In a batch processing tool, wafers are immersed as a whole unit, which highlights the need for a rear side protection layer. This layer has been usually phosphosilicate glass (PSG) that was formed during $POCl_3$ doping for the LPCVD ex-situ route (Fig. 2b). PECVD poly-Si is usually doped in-situ and therefore does not feature any dielectric protection layer (Fig. 2d). The idea is, to realize a batch removal of in-situ doped poly-Si without an additional process step using the anneal oxide that is formed in a thermal anneal process (Figs. 2c and 2e).

The aim of this work is to demonstrate the wet chemical removal of parasitically deposited poly-Si for i-TOPCon silicon solar cells by either inline or batch industrial solutions for several routes as shown in Figure 2. In a first experiment the required etching time that was needed to remove n-doped LPCVD and PECVD poly-Si was investigated on test wafer level. i-TOPCon solar cells were produced with either in-situ or ex-situ doped LPCVD poly-Si or in-situ doped PECVD poly-Si. For ex-situ doped LPCVD layers the batch wet chemical wrap-around removal is established due to high throughput and low capital cost (ITRPV [2]), but there are no reports in literature on batch wrap-around removal of PECVD poly-Si. In this study the batch poly-Si removal uses the silicon oxide layer, which is formed during annealing as a side product, for rear side masking and to avoid the need for an additional process step. After processing, the i-TOPCon cells are

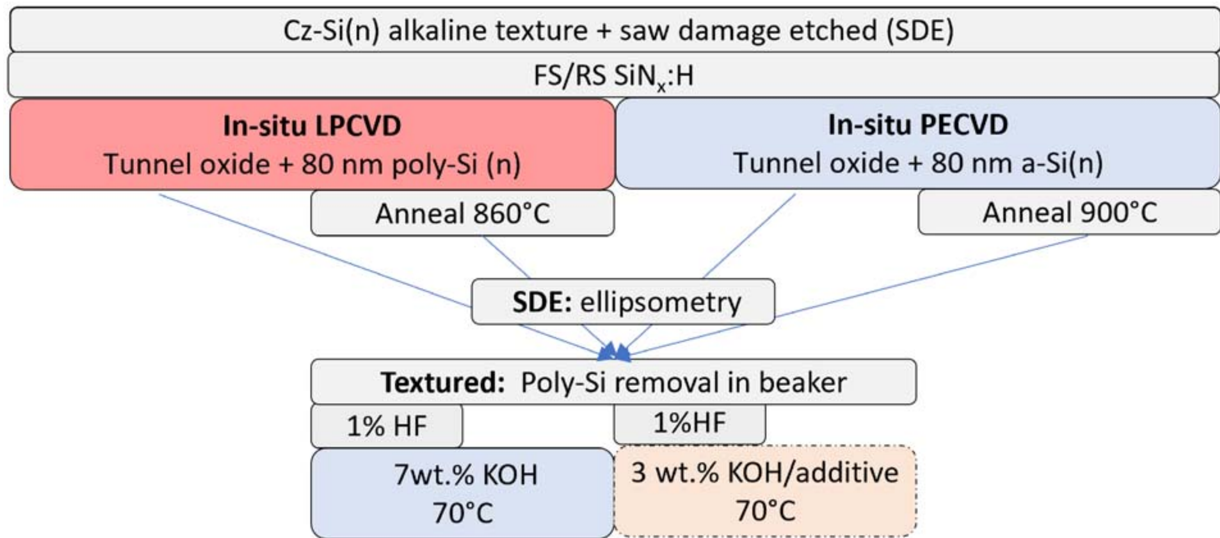

Fig. 3. Experimental matrix for poly-Si characterization on smooth saw damaged etched (SDE) samples and poly-Si removal on wafer level for textured samples.

measured at an industrial cell tester. Next to typical J–V parameters, I_{rev} at −12 V is the most important parameter with respect to describing the quality of poly-Si removal and successful edge isolation, so special focus will be put on that parameter in this paper.

2 Experimental

2.1 Removal time for poly-Si

In a pretest we measured layer characteristics of poly-Si and the required time to completely remove the poly-Si layer in heated KOH solution. The n-type Cz-Si test samples, which had been cut from processed wafers, had a size of 20×20 mm^2. The 80 nm thick LPCVD or PECVD poly-Si(n) layer was deposited on top of a 75 nm thick silicon nitride (SiN_x, Fig. 3). The poly-Si deposition was carried out in a single run, for both, saw damaged etched and textured samples. The SiN_x nitride layer below the poly-Si enhances the visibility of the polysilicon layer removal during etching (similar to Figs. 1a, 1b). SiN_x will hardly be etched by KOH and so etching will principally stop there. The temperature for LPCVD deposition was up to 600 °C, for PECVD well below 600 °C. The annealing was performed in nitrogen at 860 °C for LPCVD poly-Si and at 900 °C for PECVD a-Si. Film thickness as well as refractive index n and absorption coefficient k were determined by spectral ellipsometry and evaluated at 632 nm on saw damaged etched wafers (Tab. 1). The higher refractive index of PECVD a-Si is caused by the lower temperature during PECVD deposition, which leads to completely amorphous silicon with a large amount of hydrogen, whereas the higher temperature during LPCVD results in partially crystallized poly-Si with little hydrogen content. After LPCVD annealing, an 8 nm oxide was measured (Tab. 1).

The textured wafers with poly-Si were etched in a beaker in 3 wt.% KOH with additive and in 7 wt.% KOH at 70 °C, both with and without a 60 s 1 wt.% HF dip prior to KOH etching (Fig. 3). After the HF dip the poly-Si was hydrophobic which indicated that the oxidic layer on top of the poly-Si was fully removed. All samples were etched either until the surface was dark blue corresponding to the SiN_x layer or the samples were taken out after 600 s. The additive CellEtch by ICB GmbH & Co. KG is an additive that is usually used for alkaline edge isolation. The inspection of the removal was done visually, knowing that optically not active poly-Si cannot be seen. From the test structures described above, we cannot distinguish between full and incomplete removal on relevant samples, we indirectly determine the quality of the poly-Si removal process by fabrication of solar cells and determination of I_{rev}.

2.2 i-TOPCon solar cell process

i-TOPCon solar cells were manufactured at Fraunhofer ISE's pilot line PV-TEC on 156.75×156.75 mm^2 n-type Cz-Si wafers with a resistivity of 1.4 Ω cm. The wafers were prepared with alkaline texturing, boron diffusion, a single side borosilicate (BSG) etching in HF/HCl and batch alkaline edge isolation process followed by ozone cleaning (Fig. 4). A thin thermal tunnel oxide was grown. Then either an 80 nm n-doped LPCVD poly-Si or PECVD a-Si (in-situ), or an intrinsic 130 nm LPCVD a-Si(i) (ex-situ) were deposited with loading one wafer per slot. 130 nm was our best-known thickness for the ex-situ process. The intrinsic a-Si(i) was doped by a $POCl_3$ diffusion (12 min, 860 °C plateau temperature). The group size was 10 wafers.

To perform a poly-Si removal in a batch tool, the front side glass or oxide layer on top of the poly-Si must be removed first. For the ex-situ wafers the phosphosilicate glass (PSG) was removed on a single side etching tool

Table 1. Optical properties for as deposited and annealed in-situ doped LPCVD and PECVD poly-Si at 632 nm. Measured on a smooth surface (80 nm poly-Si deposition process for textured samples).

	LPCVD in-situ poly-Si (n)			PECVD in-situ a-Si (n)		
	n	k	Thickness (nm)	n	k	Thickness (nm)
As deposited	4.0	0.09	110	4.5	0.22	100
Annealed	3.9	0.06	98+8 nm oxide	3.9	0.06	90+8 nm oxide

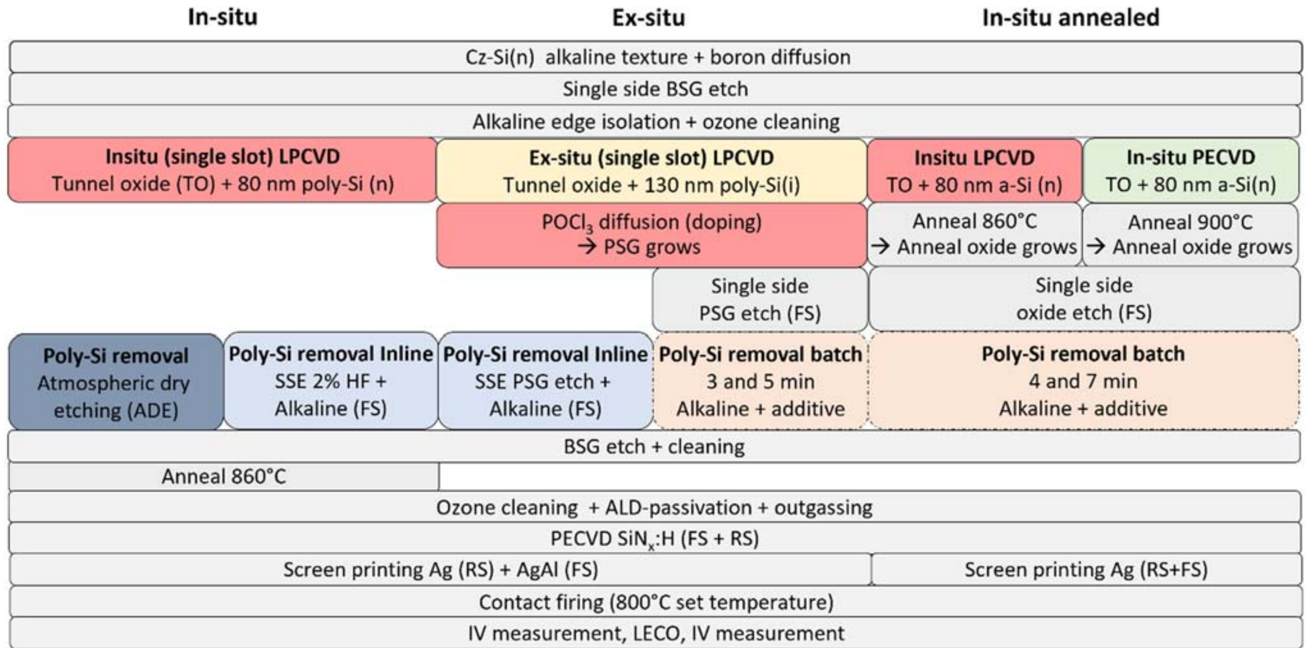

Fig. 4. TOPCon solar cell process for in-situ and ex-situ n-doped LPCVD and in-situ doped PECVD polysilicon with different poly-Si etch back processes. FS front side, RS rear side.

applying a 2% HF solution until the wrap-around was hydrophobic. For the in-situ annealed samples a 10% HF/10% HCl solution was used. The poly-Si removal was performed either in a wet chemical inline or batch tool. The inline alkaline bath was used with 7% KOH at 70 °C at a speed of 1 m/min and a bath length of 2.2 m. The batch poly-Si removal was done in 3% KOH including an additive for 3 min and 5 min for ex-situ poly-Si, and 4 and 7 min for in-situ annealed samples. The atmospheric dry etching (ADE) acted as reference [9]. A short HF dip was done before ADE to remove a native oxide layer. After the poly-Si removal, the BSG etching and cleaning followed, for the inline groups in the inline tool, for the batch groups in the batch system. The mandatory annealing step for transforming the a-Si layer to the desired final poly-Si was applied either after the poly-Si removal for the in-situ groups or after poly-Si deposition for the in-situ annealed groups. The ex-situ groups were annealed in the $POCl_3$ diffusion. The anneal plateau temperature was 860 °C for LPCVD, and 900 °C for PECVD (annealing temperatures have been optimized individually in earlier experiments). The wafers were cleaned in an ozone cleaning sequence and passivated by Atomic Layer Deposition (ALD) Al_2O_3 and subsequent outgassing and PECVD silicon nitride deposition. The screen print design was bifacial, a fast firing contact formation followed at 800 °C set temperature. The solar cells were treated by Laser Enhanced Contact Optimization (LECO) [11] and measured at an industrial cell tester under standard test condition using a flasher provided by Halm, including short time thermography and a fast hot spot evaluation [4]. The measurements were performed using a for grid touch unit on a non-reflective black chuck. The reverse bias current I_{rev} was measured at −12 V. Statistical differences for cell results are tested by t-test, significance for $p < 0.05$.

3 Results and discussion

3.1 Removal time of poly-Si

3.1.1 Influence of oxide layer removal on poly-Si removal time in KOH solution

Table 2 shows etch rates calculated from measured removal times of 80 nm LPCVD and PECVD TOPCon layers with and without oxide covering the poly-Si. In the presence of an oxide layer on top of a-Si/poly-Si layer the KOH

Table 2. Etch rate calculated from removal time of 80 nm *n*-TOPCon on textured samples on SiN_x within different KOH solutions without HF dip and with HF dip prior to KOH at 70 °C. Etching selectivity is the ratio between the poly-Si etch rate and effective etch rate (initial oxide etch rate and poly-Si etch rate).

	Crystallinity	Effective etch rate[1] w/o HF (nm/s)		Poly-Si etch rate w/ HF dip before (nm/s)		Etching selectivity	
		7% KOH	3% KOH/Add	7% KOH	3% KOH/Add	7% KOH	3% KOH/Add
LPCVD							
As deposited	poly-Si	1.6	0.7	8.0	8.0	5:1	12:1
Annealed	poly-Si	0.5	<0.1	4.0	4.0	8:1	>30:1
Ex-situ [2,3]	poly-Si			10 [2]	16 [3]		
PECVD							
As deposited	a-Si	1.1	0.3	4.0	2.7	4:1	8:1
Annealed	poly-Si	0.4	<0.1	2.0	2.0	6:1	>15:1
As deposited[4]	a-Si			7 [4]			

[1]Initial oxide and poly-Si etch rate.
[2]0.5−1% KOH at 60−70 °C [5].
[3]KOH:polish additive:H_2O = 5:3:80 at 70−80 °C [5].
[4]70 °C at 7% KOH [1].

solution with additive ends up with a lower effective etch rate compared to the higher concentrated KOH without additive. Here, the effective etch rate includes the initial low oxide etch rate of the silicon oxide as well as the higher etch rate of poly-Si in KOH. However, if the surface anneal oxide is removed by a HF pre-treatment we see the poly-Si etch rate being equal for both solutions. This finding shows the working principle of the additive which reduces the etch rate for the hydrophilic surface (anneal oxide) and results in an etching selectivity of up to >30:1 for annealed poly-Si (Tab. 2). The etching selectivity is the ratio between the poly-Si etch rate and effective etch rate (initial oxide etch rate and poly-Si etch rate. This effect agrees with poly-Si removal for ex-situ doped poly-Si [5] where an etch rate for n-doped LPCVD poly-Si of 16 nm/s is found and for PSG of 0.1 nm/s in KOH with polish additive, respectively. So, the anneal oxide seems to be sufficiently resistant to retard etching of the poly-Si layer in KOH. In diluted KOH without additive etch rates are reported for n-doped LPCVD poly-Si of 10 nm/s [5] for n-doped PECVD poly-Si of 7 nm/s [1]. Our calculated etch rates might be lower than literature data due to a different additive or experiment design with removal time and the determination of the end point of when etching effectively stops. At the end, sometimes poly-Si residues remained on the wafer as stains in the center of the wafer.

Two conclusions can be drawn from these findings: (i) an oxide removal before KOH etching is necessary to achieve proper etch rates for poly-Si removal and (ii) the application of an additive based KOH solution allows a lower effective etch rate of poly-Si in the presence of a surface oxide. These conclusions of boostered etching selectivity of an additive based KOH solution for poly-Si layers with or without surface oxide can be exploited in TOPCon solar cell production.

3.1.2 Exploiting etching selectivity in industrial poly-Si wrap-around removal process

Two strategies for an efficient removal of poly-Si wrap-around for industrial TOPCon solar cell production will be discussed in this paper: (1) the inline single side etching and (2) the combination of a single side oxide removal and subsequent batch processing, both of which result in a single sided poly-Si wrap-around removal.

The inline process etches only the front side, which is in contact with the etching solution, and which therefore does not need etching selectivity nor additive. This process must be used for as-deposited poly-Si since the etching selectivity between hydrophobic and hydrophilic surfaces is not sufficient in this case, and an alternative batch process would damage the TOPCon layer. A HF dip prior to KOH processing reduces the required KOH etching time for poly-Si by a factor of five because the HF treatment has already removed the oxidic layer and KOH can directly attack the poly-Si layer. Thus, for inline poly-Si etching an HF dip is suggested prior to KOH etching to increase tool throughput, and doing so an efficient etch back of the poly-Si wrap-around can be achieved.

Batch processes for wet chemical etching allow a high throughput and cost-efficiency in industrial solar production. The etching selectivity discussed above can be exploited to achieve a single side etching in a batch tool where the solar cell precursor is fully immersed. This can be done by applying a single side HF dip on the side with the parasitic poly-Si wrap-around leaving this side without oxide and the other side with surface oxide on the full area TOPCon layer. If this wafer is subsequently fully immersed in an additive based KOH solution (batch tool) this ends up with a high etch rate for the oxide-free side with the parasitic poly-Si and a low etch rate for the TOPCon side, which is protected by the oxide layer.

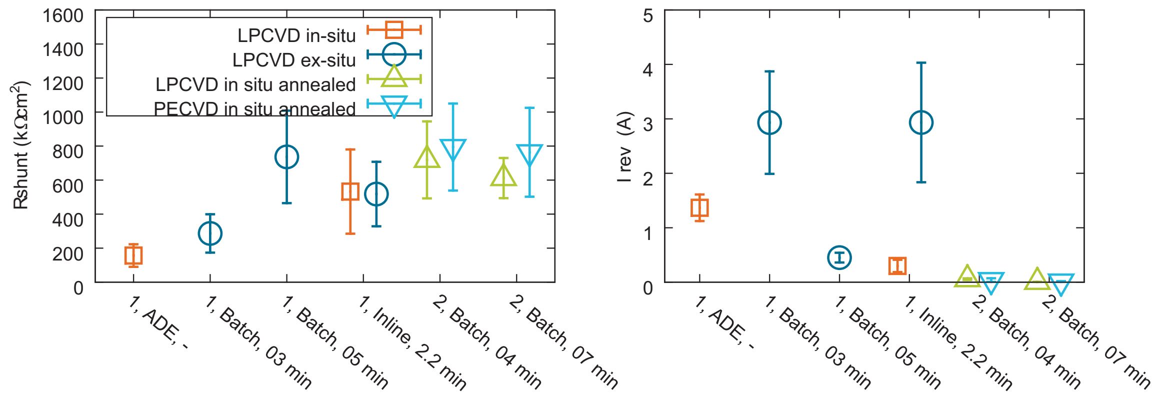

Fig. 5. Reverse bias current I_{rev} at −12 V for i-TOPCon solar cells (n-type Cz-Si, M2) with LPCVD in-situ and ex-situ doped poly-Si and with "in-situ annealed" LPCVD and PECVD with different poly-Si removal processes: ADE – atmospheric dry etching, alkaline batch process and alkaline inline process. Mean ± standard deviation.

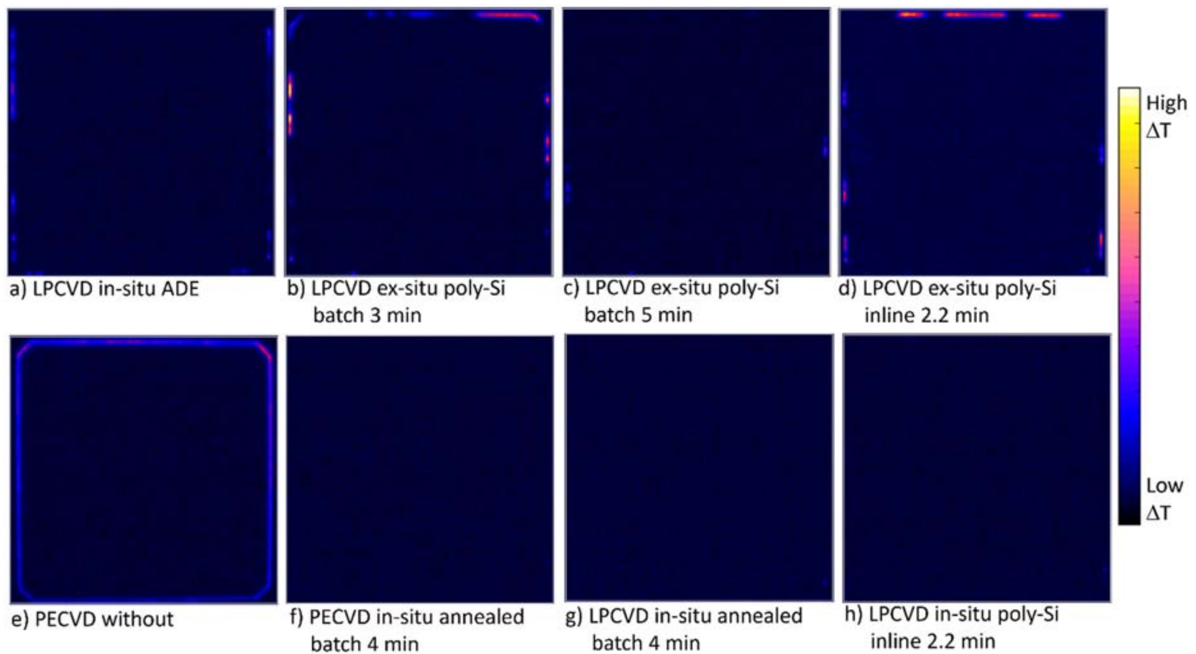

Fig. 6. Thermography images taken under reverse voltage (−12 V) for i-TOPCon solar cells with PECVD in-situ and LPCVD in-situ and ex-situ doped poly-Si(n) wrap-around removal by (a) ADE (b,c, f, g) alkaline batch, (d, h) alkaline etching and (e) without poly-Si wrap-around removal. 156 × 156 mm^2. Thermography images show a temperature increase where current flows under reverse conditions.

3.2 LPCVD and PECVD i-TOPCon solar cell results

3.2.1 Reverse *IV* characteristic and thermography

Figure 5 shows the shunt resistance R_{shunt} and the reverse current I_{rev} at −12 V of the fabricated i-TOPCon solar cells. For ex-situ doped poly-Si both the 2.2 min long inline process as well as the 3 min long batch poly-Si removal process allow for R_{shunt} values of 300–500 kOhm cm^2 determined around $V = 0$ V, but also a rather high I_{rev} over 2 A in reverse direction at $V = -12$ V (Fig. 5). Nevertheless, these I_{rev} values are lower than corresponding I_{rev} values without poly-Si removal for 30–100 nm PECVD poly-Si (3 to 10 A, −12 V) [4] and as high as the KOH polish batch poly-Si removal process for LPCVD layers, which resulted in 3 A at −14.5 V [5]. In general, high I_{rev} values bear the risk of hot-spot generation in PV modules manufactured with these cells, and thus can lead to damaged modules. These high reverse currents can be seen as bright edges in thermography images e.g. for ex-situ doped poly-Si (Figs. 6b and 6d). These bright edges translate to a local temperature increase at the edges under reverse bias voltage caused by a current flow. Without wrap-around removal the temperature increase surrounds the cell (Fig. 6e). Is a wrap-around removal performed, the bright lines are interrupted or disappear completely, just as for example Figure 6f.

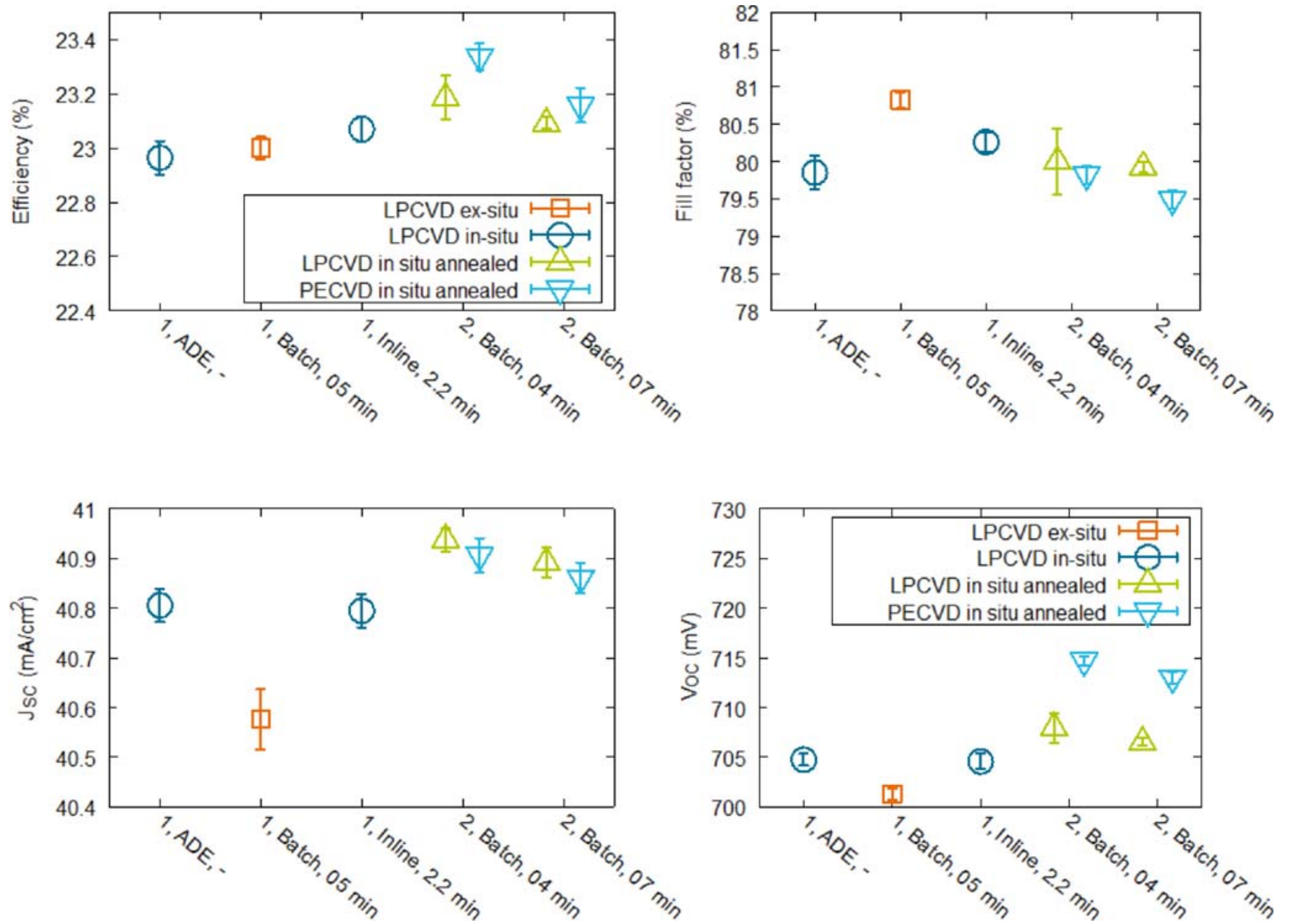

Fig. 7. IV parameters for i-TOPCon solar cells (n-type Cz-Si, M2) after LECO treatment for a first experiment (1) with LPCVD in-situ and ex-situ doped poly-Si and for a second experiment (2) with "in-situ annealed" LPCVD and PECVD layers. Poly-Si wrap-around removal has been achieved applying ADE (atmospheric dry etching), alkaline batch or inline processes. Mean ± standard deviation.

Apparently, in the case of the 130 nm ex-situ doped poly-Si, the short inline and batch etching times are not sufficient to remove the edge related shunt completely. The KOH etching times for poly-Si removal in our experiment exceed the expected etching times of less than one minute for poly-Si from the pretest. This might be due to an insufficient PSG removal during the 2% HF inline process prior to hot KOH and which as a result prevented a high-quality etching process of the front poly-Si layer. The "in-situ annealed" LPCVD and PECVD poly-Si samples were treated with 10% HF/10% HCl for single side anneal oxide removal and lead to the lowest I_{rev} in the experiment of less than 0.1 A at −12 V. These values are as low as LPCVD TOPCon cells with poly-Si removal with HF/HNO_3 followed by KOH with values of 0.15 A at −14.5 V [5]. For ex-situ doped LPCVD poly-Si a longer batch poly-Si removal process of 5 min batch in KOH reduced I_{rev} to 0.5 A, and thus to considerably lower values than described above. For in-situ doped LPCVD poly-Si layers, inline poly-Si removal processing resulted in a low $I_{\mathrm{rev}} = 0.3$ A. As a result, several of these wet chemical poly-Si removal processes lead to a lower reverse current than the ADE process. The reason might be that the ADE process had originally been optimized for slightly rougher rear surfaces after acidic single side boron diffusion etching [9]. To sum up this section for several TOPCon processing routes, there are industrial wet chemical etching solutions available that allow low I_{rev} values, but the choice depends on the actual process sequence not all possible combinations are meaningful.

3.2.2 Solar cell efficiency

Figure 7 shows the IV results for TOPCon solar cells for groups with low I_{rev}. It is noteworthy that the solar cells have been fabricated in two consecutive experiments, which is highlighted by "1" on the x-axis for the first experiment, and "2" for the second, correspondingly. In the first experiment, in-situ and ex-situ LPCVD poly-Si have been tested, and both inline and batch wet chemical poly-Si

etching lead to solar cell efficiencies of 23%. Here, 130 nm thick ex-situ doped poly-Si layers result in lower J_{sc} values than 80 nm thick in-situ doped poly-Si layers, which results in increased parasitic absorption on the rear side [13]. The highest fill factor (FF) was found for ex-situ doping. Whereas $V_{oc} = 705 \pm 0.9$ mV was measured for inline poly-Si removal and in-situ doping, $V_{oc} = 701 \pm 0.6$ mV was found for ex-situ poly-Si with batch poly-Si removal, which we expect to be a result of the lower level of process optimization for the ex-situ route, as our standard sequence uses in-situ doped LPCVD layers.

For the second experiment, we prepared "in-situ annealed" TOPCon cells with LPCVD and PECVD poly-Si layers and the same thickness of 80 nm. This time, we decided to remove the poly-Si wrap-around only by etching in a batch tool and here we see an even higher J_{sc} and V_{oc} than for all other groups. In this experiment, we used a silver paste on the front side which increased to $V_{oc} = 715 \pm 0.5$ mV for 4 min batch wrap-around poly-Si removal process compared to the use of a silver/aluminum paste in experiment 1 ($V_{oc} = 705 \pm 0.9$ mV). Values are given as mean ± standard deviation. Compared to this, a longer poly-Si removal time of 7 min reduced all *IV* parameters due to slightly damaging the anneal oxide. For a 4 min batch wrap-around poly-Si removal process, we find a I_{rev} at −12 V lower than 0.1 A and a solar cell efficiency of 23.4%.

4 Conclusion

The aim of this work was to identify an industrially feasible etch back process sequence with low processing time and uniform etch back quality for the removal of parasitic poly-Si wrap-around in i-TOPCon solar cells. The poly-Si removal study on wafer level showed that an HF dip prior KOH etching reduces the required KOH etching time by the factor of at least five since the HF removes any oxide on top of the poly-Si and allows for faster attack of the etchant to the poly-Si layer. An additive in the KOH solution enhanced etching of HF treated poly-Si (hydrophobic) and protected the untreated poly-Si/oxide (hydrophilic). Transferred to the solar cell it means that the selective etching between rear and front side in KOH/additive is high enough to realize a batch cluster process for etching annealed poly-Si.

i-TOPCon silicon solar cells were fabricated with in-situ and ex-situ LPCVD n-doped poly-Si and different poly-Si removal processes. The in-situ LPCVD sequence was successful with an inline polysilicon removal in hot KOH, the ex-situ LPCVD sequence with a batch cluster polysilicon removal process. Both inline and batch wet chemical poly-Si etching result in low I_{rev} values and efficiency of 23.2%, however, inline polysilicon removal for the ex-situ route needs to be optimized further. In a follow-up experiment, i-TOPCon solar cells with "in-situ annealed" LPCVD and PECVD poly-Si were fabricated in a shorter sequence. A batch poly-Si removal process was applied successfully, highlighted by I_{rev} of <0.1 A and a solar cell efficiency of 23.4%.

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Conflicts of interest

The authors have nothing to disclose.

Data availability statement

This article has no associated data generated. Data associated with this article cannot be disclosed due to other reason.

Author contribution statement

All authors state that they contributed equally to the paper.

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