EPJ Photovoltaics **4**, 45108 (2013)
www.epj-pv.org
DOI: 10.1051/epjpv/2013019

Laser annealing of thin film polycrystalline silicon solar cell

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Received: 18 September 2012 / Accepted: 11 April 2013
Published online: 13 November 2013

Abstract Performances of thin film polycrystalline silicon solar cell grown on glass substrate, using solid phase crystallization of amorphous silicon can be limited by low dopant activation and high density of defects. Here, we investigate line shaped laser induced thermal annealing to passivate some of these defects in the sub-melt regime. Effect of laser power and scan speed on the open circuit voltage of the polysilicon solar cells is reported. The processing temperature was measured by thermal imaging camera. Enhancement of the open circuit voltage as high as 210% is achieved using this method. The results are discussed.

1 Introduction

The past few years have seen an extensive use of rapid thermal processing (RTP) by means of halogen lamps in semiconductor technology for dopants activation, surface oxidation and for defects annealing of polycrystalline silicon on glass. On one hand, the RTP process is widely used for the crystallization of amorphous silicon on glass for solar cells and thin film transistors (TFTs) applications [1–5]. On the other hand, RTP on polycrystalline silicon materials can also be used to reduce the point defects present in the poly-Si layers and to activate the dopant elements [1, 2, 6–8]. However this method fails to achieve temperatures above 950 °C for long time (>1 min) while keeping the borosilicate glass substrate intact. Using laser thermal annealing (LTA), it is possible to achieve very high temperature very close to the melting point of crystalline silicon for few seconds with minimal or negligible deformation of borosilicate glass substrate. In this work we study the laser treatment of polysilicon solar cells in the solid phase regime and the consequence on their photovoltaic parameters.

Structures composed of Glass/SiON/SiN/N+/P-/P+ were routinely made by CSG Solar Pvt. Ltd. of Sydney, Australia [9]. The deposited stack on textured glass substrate employing plasma enhanced chemical vapour deposition (PECVD) is followed by solid phase crystallization at 600 °C. The defect passivation and dopant activation of un-activated dopants were done by rapid thermal annealing at around 940 °C using halogen lamps. A plasma hydrogenation tool is used in the end to passivate the defects completely. Although 10% efficiency is quite good, simulations show an efficiency potential of 12−13% with the present structure if the defects are more efficiently passivated. As the rapid thermal annealing process is already at its extreme before softening the glass, laser induced annealing may provide an alternative solution. The aim of this work is to anneal the polycrystalline silicon cell structure [10] composed of Glass/SiON/SiN/N+/P-/P+ at the highest temperature possible but below the melting point of silicon, in order to reduce the defect and to activate more dopants without damaging the stacked structure. For the study the polycrystalline silicon structures were made on planer glass substrates instead of textured glass substrates.

2 Experimental details

The samples used for laser annealing are deposited on planar borosilicate glass substrate. The structure of the samples is Glass/SiON/SiN/N^+/P^-/P^+ where the different layers were deposited by the Plasma Enhanced Chemical Vapor Deposition method. The annealed final structure is shown in Figure 1. The amorphous silicon $N^+/P^-/P^+$ stack was solid phase crystallized (SPC) prior to laser annealing. The laser source used for annealing is manufactured by LASERLINE Inc. and it is composed of a dual high power laser system simultaneously emitting at wavelengths of 808 nm and 940 nm. The maximum total power in the source is 3 kW.

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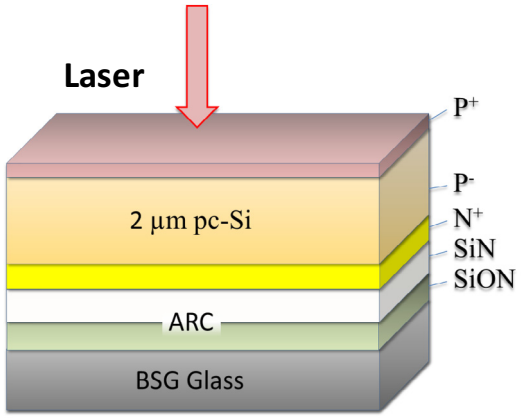

Fig. 1. Schematic diagram of the sample.

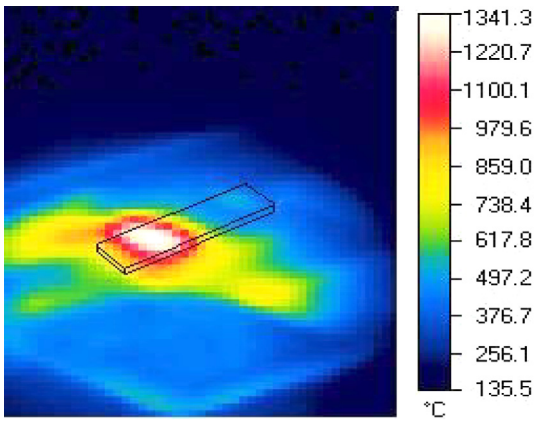

Fig. 2. Infrared imaging of temperature variation during laser annealing. The sample is schematically indicated as a rectangular object.

Using a special setup the laser was made to incident on the sample in a shape of line with dimension of ∼5 cm × 0.4 cm. The relative speed of the sample perpendicular to the laser line was varied from 10 cm/min to 30 cm/min. The laser power at the source was varied from 0.5 to 3 kW, but it should be noticed that there is always a ∼33% optical laser power loss before reaching the sample surface in addition to loss due to reflection from sample surface. In all cases a substrate heater was used to elevate the sample temperature around 430 °C to enhance the light absorption in silicon and to reduce the thermal expansion coefficient mismatch between the substrate and the silicon layers.

During laser processing a thermal imaging camera named M7600PRO from Mikron Infrared Inc. was used extensively to monitor the thermal profile in each point of the sample. Figure 2 shows a captured image from a video sequence. The sample is schematically indicated as a rectangular object. The temperature estimation depend on the emissivity constant of the surface of the P^+ Si top layer and it is very tricky to find the exact values at 1000−1500 °C due to a possible phase change at some parts of the silicon layer. Using suitable emissivity factors, the maximum processing temperature was estimated with ±30 °C error in the 1000−1500 °C range.

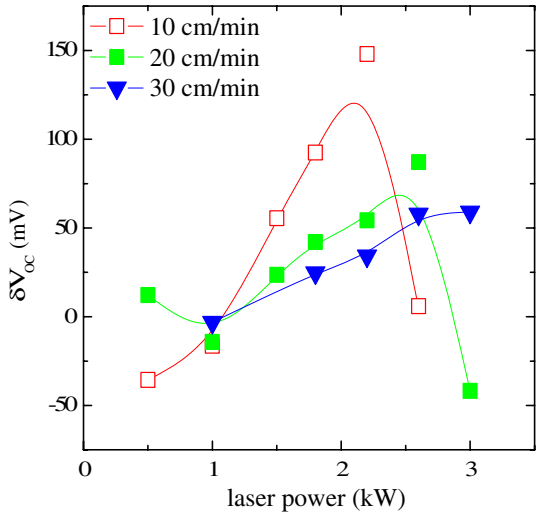

Fig. 3. Variation of open circuit voltage of laser annealed polysilicon structures as a function of laser power and at different scan speeds.

The open circuit voltage of the cell structure, before and after laser processing, was measured using the Suns-V_{OC} setup manufactured by Sinton Pvt. Ltd. [10]. Prior the measurements, the sample were etched at the corner to remove the P^+ and P layers, and to have access to the N^+ region. Electron Back Scattering Detraction (EBSD) experiment was also done to observe the presence of grain distribution with different laser annealing conditions.

3 Results and discussions

The samples were annealed by line shaped laser spot at different scan speeds and power densities. Figure 3 shows the variation of the open circuit voltage (V_{oc}) versus the operational parameters. Before laser annealing the open circuit voltage of the polysilicon structure was 130 ± 5 mV measured. The general observed trend is an increase of V_{oc} as the laser power increases and then a decrease above a certain power threshold. It is found that this threshold depends on the applied scan speed. The higher the scan speed, the higher is the power density needed reach this threshold. Later it will be seen that this threshold indicates the melting point of crystalline silicon. As a result, V_{oc} goes through an optimal value for each scan speed. A maximum V_{oc} value of 280 mV was obtained for a polysilicon structure annealed at 2.2 kW laser power and a scan speed of 10 cm/min. This indicates an enhancement of the V_{oc} of about 150 mV due to the laser annealing. Another noticeable result is that at very low power densities of 0.5 kW and scan speed of 10 cm/min, V_{oc} of the samples is lower than its original value of 130 ± 5 mV. This might be due to some defects (dislocations) induced by laser processing. These results indicate that benefit of laser applied to such structures is strongly dependent on the thermal budget assigned to the sample.

A thermal imaging camera was used to monitor the laser annealing process at different power and scan

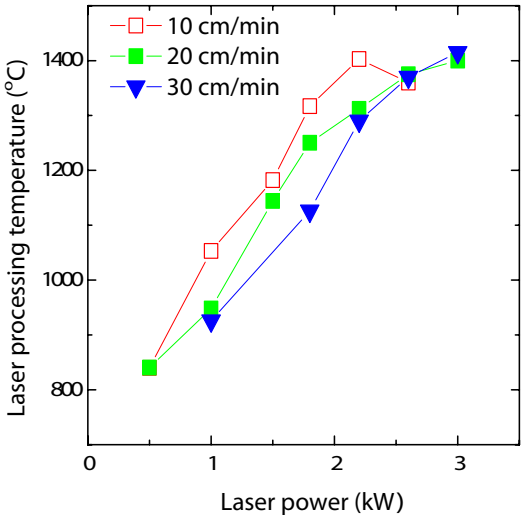

Fig. 4. Variation of processing temperature with respect to variation of laser power at different scan speed.

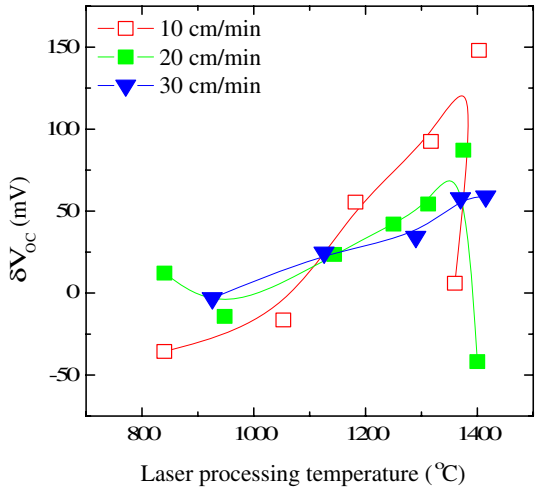

Fig. 5. Open circuit voltage of laser annealed polysilicon structures as a function of processing temperature.

speed. The corresponding temperatures were estimated. From Figure 4 it is observed that the sample temperature is monotonically increasing with laser power during annealing. A maximum temperature of ∼1410 °C, that is the melting point of polycrystalline silicon, was reached for a 2.2 kW laser power and 10 cm/min laser scan speed. As a substrate heater was used to set the sample temperature to 430 °C prior to laser processing, a processing temperature around 840 °C was obtained for only 500 W of laser power. Due to optical loss in the laser processing system and further losses with reflection from the sample itself, only around 200 W of laser power is incident on ∼5 cm × 0.4 cm area of sample. This indicates the effectiveness of the substrate heater in terms of direct elevation of sample temperature. Pre-heating the substrate increases the optical absorption coefficient which in turns helps the poly-silicon layers to absorb more efficiently the infrared laser power. The substrate temperature around 430 °C also helps to reduce the severe stress in glass-silicon interface by lowering the mismatch of thermal expansion coefficient of poly-silicon and glass substrate during high temperature laser processing.

Figure 5 plots the variation of V_{oc} as a function of processing temperature. The trend is similar for samples processed at different scan speed, first a steady increase in V_{oc} and then an abrupt decrease for processing temperatures around 1410 °C which is close to melting point of crystalline silicon. It is also observed here that for a similar processing temperature over 1200 °C, δV_{oc} is inversely proportional to the scan speed. This is indicating that higher duration of elevated temperature is beneficial for defect annealing and or dopant activation. It may also occur that a shorter duration of annealing is hampering the polysilicon layers to attain a stable structure before the cooling down.

Figure 6 shows the EBSD images of samples before and after laser processing. The non annealed polysilicon structure (Fig. 6a) has grains in the range 1−5 microns in diameter. From Figure 6b it is obvious that laser thermal annealing did not affect the grain sizes or the distribution, while the open circuit voltage enhanced by 150 mV as reported above. Such improvement can therefore be only possible to a reduction in defects and/or to an electrical activation of dopants in the absorbing p layer. At 10 cm/min scan speed, further increase in laser power to 2.6 kW changes the grain structure completely and shows clear pattern of recrystallization (Fig. 6c). This recrystallization is also responsible for the sudden drop in open circuit voltage observed in Figure 3.

Some samples, on which EBSD study was performed, were also undergone SIMS experiment to monitor the boron and phosphorus distributions of the $p^+p^-n^+$ structure. Figures 7a and 7b plots respectively the boron and phosphorus profiles of reference and laser annealed sample at 2.2 KW. The B and P profiles of the non annealed sample are sharp and the junctions are well defined. After annealing, the boron and phosphorus profiles are graded and the elements are penetrating the p^- region from both sides. The B and P surface concentrations are lower than those of the reference sample and the corresponding junction depths are deeper. These results indicate that the B and P diffuse towards the volume probably in a sub-melting regime. Indeed despite the short time of the process (the scan speed is 10 cm/s) the dopants diffusion occurs thanks to the very high temperature process. The process can be compared to the annealing by flash lamps [11] here we offer temperatures above 1200 °C. yet the reconstruction of the layers after annealing is very good as witnessed by the EBSD images and by a higher open circuit voltage value obtained for this sample as compared to that of the reference. Increasing the laser power up 2.6 kW resulted in a strong distribution of the dopants (not shown here) within the $p^+p^-n^+$ structure and therefore to less defined junctions. As a consequence, a lower open circuit voltage is measured on this sample.

To complete our study, we have prepared 16 solar cell $p^+p^-n^+$ structures and post-annealed them using halogen

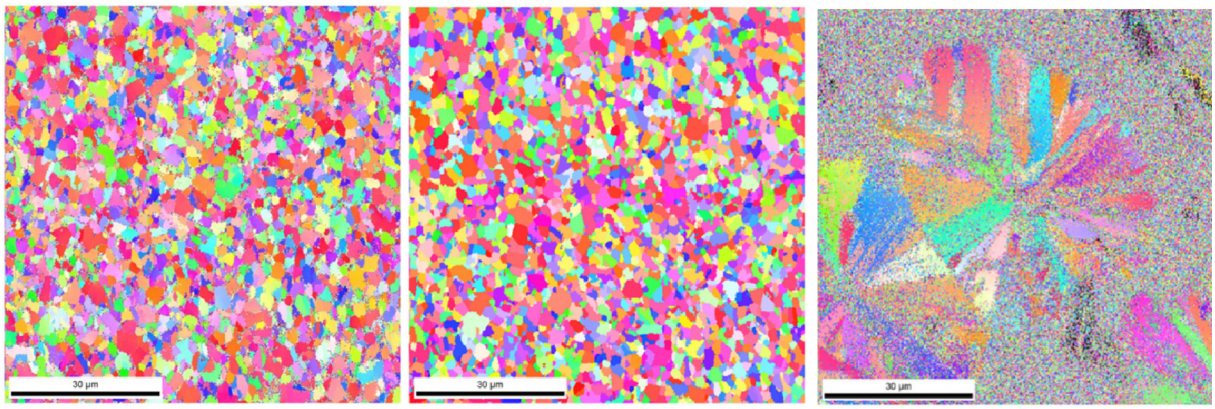

Fig. 6. EBSD images of samples (a) before laser processing, (b) 2.2 kW, 10 cm/s, (c) 2.6 kW, 10 cm/s.

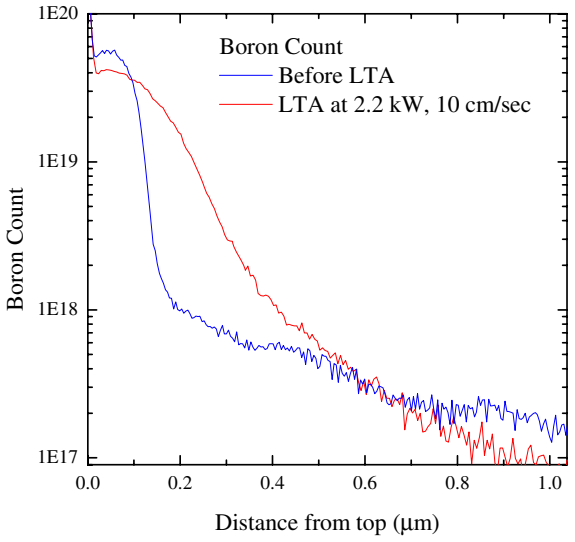

Fig. 7. SIMS study on the samples before and after LTA: (a) boron count, (b) phosphorus count.

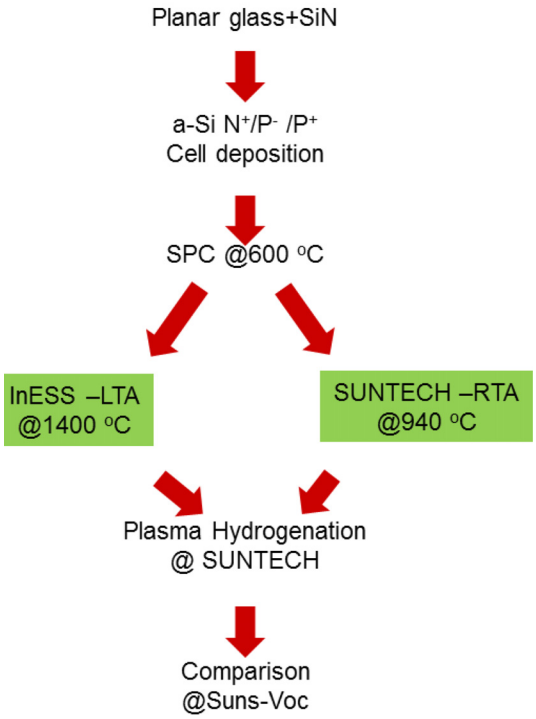

Fig. 8. Schematic diagram of experiment for LTA and RTP comparison.

Table 1. Laser annealing and rapid thermal annealing comparison.

	$V_{oc}(1)$	p_{FF}	p_{Eff}
LTA	480	76.6	7.3
RTA	463	75.5	7.0
Improvement by LTA	+3.6%	+1.4%	+4.3%

lamps (RTA) at Suntech Pty, Australia or CW IR laser (LTA) at ICube lab before to make contacts. The same hydrogenation step was applied to all cells. The open circuit voltage of these cells was measured using the SunsVoc system and the results are displayed in Table 1. An average

open circuit voltage of 480 mV was measured after LTA, which is 17 mV higher than for RTA processed cells. Assuming a current density of the cells at 20 mA/cm^2, we found that the open circuit voltage, the pseudo fill factor and the pseudo efficiency are enhanced by 3.6%, 1.4% and 4.3% as compared to the values of the RTA annealed cells. While the hydrogenation step was previously thoroughly optimized for the routinely made RTA annealed structures [12], it is not the case for the LTA cells. Thus higher cells performances are expected for the late samples. Overall the LTA process shows its effectiveness in defect passivation when compared to the conventional RTA.

4 Summary

Polysilicon solar cells structures were CW laser irradiated in the sub-melting regime. We have demonstrated a 210% improvement in V_{oc} by using a fast laser scanning. A further enhancement in V_{oc} is possible by a suitable plasma hydrogenation process. Using LTA process and plasma hydrogenation a high open circuit voltage of 480 mV obtained, which is 17 mV higher when LTA is replaced by conventional RTA using halogen lamps. Similarly, in addition to improvement of pseudo fill factor, the pseudo cell efficiency also increases by 3.6% when the LTA process is applied to the cells. The increase of open circuit voltage after laser thermal annealing is probably due to passivation of defects and/or activation of the dopants. For annealing at power below 2.2 KW, the process is in sub-melt region of polycrystalline silicon and seemly the grain structures are not affected despite the high temperature processing beyond 1200 °C for a very short time. Above the melting point of polycrystalline silicon which occurs for high laser power, both boron and phosphorus dopants diffuse in the layers resulting in non defined junctions and therefore in low open circuit voltage values. At processing temperature below 1000 °C, the open circuit voltage of the cells is lowered due to laser induced defects created by sudden change in temperature. These results show that the improvement of the open circuit voltage during laser thermal annealing is a result of a tread-off between thermal defect annealing and defects formation.

This work was funded by the European commission under project entitled POLYSIMODE.

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Cite this article as: A. Chowdhury, A. Bahouka, S. Steffens, J. Schneider, J. Dore, F. Mermet, A. Slaoui, Laser annealing of thin film polycrystalline silicon solar cell, EPJ Photovoltaics **4**, 45108 (2013).