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Thin film pc-Si by aluminium induced crystallization on metallic substrate

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Abstract Thin film polycrystalline silicon (pc-Si) on flexible metallic substrates is promising for low cost production of photovoltaic solar cells. One of the attractive methods to produce pc-Si solar cells consists in thickening a large-grained seed layer by epitaxy. In this work, the deposited seed layer is made by aluminium induced crystallization (AIC) of an amorphous silicon (a-Si) thin film on metallic substrates (Ni/Fe alloy) initially coated with a tantalum nitride (TaN) conductive diffusion barrier layer. Effect of the thermal budget on the AIC grown pc-Si seed layer was investigated in order to optimize the process (i.e. the quality of the pc-Si thin film). Structural and optical characterizations were carried out using optical microscopy, μ-Raman and Electron Backscatter Diffraction (EBSD). At optimal thermal annealing conditions, the continuous AIC grown pc-Si thin film showed an average grain size around 15 μm. The grains were preferably (001) oriented which is favorable for its epitaxial thickening. This work proves the feasibility of the AIC method to grow large grains pc-Si seed layer on TaN coated metal substrates. These results are, in terms of grains size, the finest obtained by AIC on metallic substrates.

1 Introduction

Compared to classical photovoltaic technologies based on bulk crystalline silicon, thin film approach enables to reduce the material consumption drastically. Furthermore, it allows large area deposition on low-budget foreign substrates. Thus, thin film polycrystalline silicon (pc-Si) solar cells on non-silicon substrates are interesting to reduce the cost of photovoltaic electricity provided high quality silicon is produced and efficient optical confinement is applied.

As substrate's candidates, ceramic or glass ceramic insulating materials have been previously suggested [1–3] Nevertheless, metallic foils can offer similar and additional advantages. They are cheap, thermally stable and flexible thus they can be rolled. Several material technologies have been proposed to obtain pc-Si thin films on metallic substrate. Some technologies consist in using buffer and template layers on an metallic substrate for the hetero-epitaxial growth of large-grain (20-50 μm) silicon thin films (2–10 μm) [4, 5]. However, these approaches do not take profit of the metal substrate conductivity. Hence, the theoretical efficiency of such cells will be strongly limited by an important shadowing effect due to the inter-digitated contact configuration. Another technology consists in the direct deposition of crystalline silicon films produced by standard plasma processes at low temperature. The metal substrate directly plays the role of the back-contact in a double-side contact configuration cell. Efficiency up to 5.8% has been reported [6]. However, the size of the Si crystallites are relatively small (<1 μm) which limited the improvement of the electronic quality of the Si thin films thus obtained. One attractive method to produce pc-Si solar cells consists in thickening by epitaxy a large-grained seed layer. Large grains p-type pc-Si can be obtained by aluminum induced crystallization (AIC) [7]. Thin-film polycrystalline-silicon solar cells based on AIC and thermal CVD with 8% efficiency has already been reported on alumina substrate [8].

In the present work, aiming to exploit simultaneously the advantages of the AIC method and metallic substrates, the feasibility of AIC process on a metallic substrate is investigated. The AIC method is a relatively simple process, which enables a low thermal budget and a much shorter crystallization time compared to solid phase crystallization activated by classical annealing. To avoid any diffusion of metallic impurities from the substrate during the process, a tantalum nitride (TaN) conductive diffusion barrier layer has been used. The annealing temperature and time are the key parameters of the Al/Si exchange process. Thus, the thermal budget influence on the pc-Si film quality was studied for optimizing the AIC process on metallic substrate coated by TaN.

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Table 1. AIC thermal budget parameters.

Sample id.	Temperature (°C)	Time (h)
S.1	450	16
S.2	475	16
S.3	500	8
S.4	525	4
S.5	550	2

2 Experiment details

Metallic foils of 5×5 cm^2 made of ferritic steel (from APERAM Inc.) were used as substrates. Because the substrate's roughness can modify the nucleation rate [5, 6], it has a major influence on the crystallographic quality of the AIC grown pc-Si layers. Therefore, the substrates with the minimal roughness achievable were used. Surface maps have been realized by WYKO NT9100 surface profiler on the substrates prior to the deposition of TaN layers. An average roughness of 255 nm has been measured on a representative sample. This controlled surface roughness is favorable to the AIC process [9]. The metallic substrates were coated with a 1 μm thick cubic face-centered TaN layer deposited by sputtering. Afterwards, as a precursor in the AIC process, aluminium layer (200 nm thick) was deposited by e-beam evaporation (EBE). The samples were then exposed to air for 1 week prior to amorphous silicon (a-Si) deposition in order to achieve an AlO_x permeable membrane. This membrane is essential for a successful layer exchange [10]. Afterward, the AlO_x/Al layers were coated with radiofrequency magnetron sputtered a-Si (400 nm).

Then, the samples were annealed in a quartz tube furnace under nitrogen gas flow. The investigated temperature range was chosen above the threshold crystallization temperature of a-Si in contact with aluminium and below the eutectic temperature (Al/Si; $T_{eu} = 577$ °C). By considering that for lower temperature annealing the incubation time (characteristic time needed to form the first nuclei) is longer than for higher temperature, the thermal budget was compensated by extending the annealing time. However, a maximum time of 16 h was fixed in a partial way in order to limit the duration of the whole process. The parameters used to optimize the AIC annealing are reported Table 1.

After annealing, a residual layer composed of aluminium and silicon islands on the top of the pc-Si surface is formed. This layer was removed by an appropriate chemical etching or mechanical polishing. A schematic illustration of the AIC process on these samples is reported in Figure 1.

The resulting p-type (Al) pc-Si thin films obtained were analyzed with a Renishaw RAMASCOPE 2000 μ-Raman spectrometer using the 633 nm excitation wavelength of a HeNe laser. The crystalline fractions were evaluated from the optical microscope observations. The crystal orientation and grain size analysis were carried out by SEM LEO 1530 using the electron backscatter diffraction (EBSD) configuration.

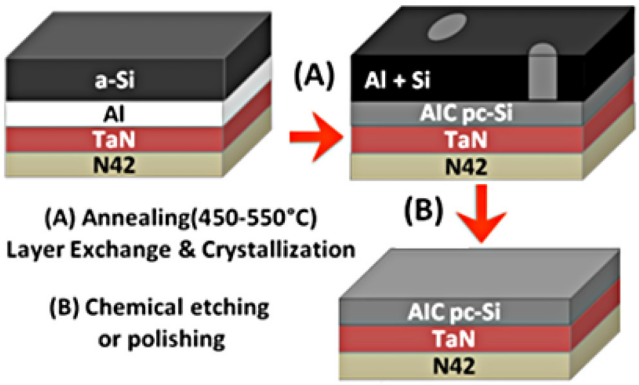

Fig. 1. Schematic illustration of the AIC process on metallic substrate.

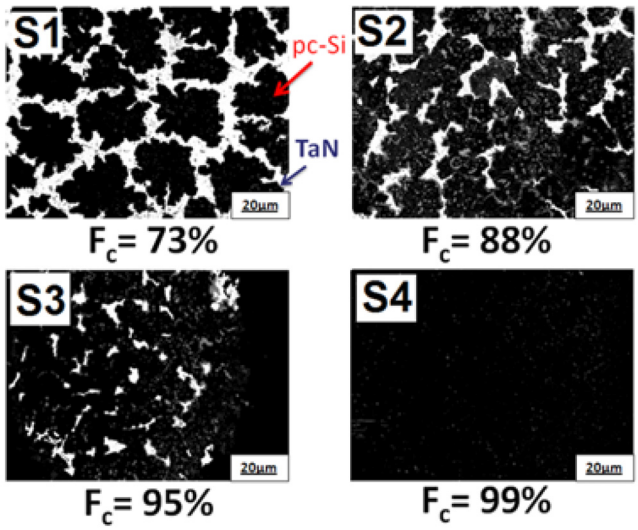

Fig. 2. Optical microscope images of AIC grown pc-Si layer after annealing and chemical etching of the residual Al/Si layers. The images were processed by a grey level converter in order to estimate the crystallized fraction (F_c).

3 Results and discussions

3.1 Grains surface coverage

After annealing, the residual Al/Si top layer was removed by chemical etching. Hence, the samples were analyzed by optical microscope. The surface images of the AIC-grown pc-Si are reported in Figure 2. The images were consecutively converted in high contrasted gray level and filtered in order to estimate the crystallized fraction (F_c).

On these images, the surface coverage of the silicon crystallites on the top of the TaN layer is clearly visible. The crystallized fraction can be described by the analysis of the grains surface coverage of the optical microscope images. The resulting values are reported under each image on Figure 2. The crystallized fractions increase from S1 to S5. It reaches 73% for S1 while it is closed to 100% for S4 and S5 (S5 is not shown here as it is similar to S4). The crystallization is almost completed

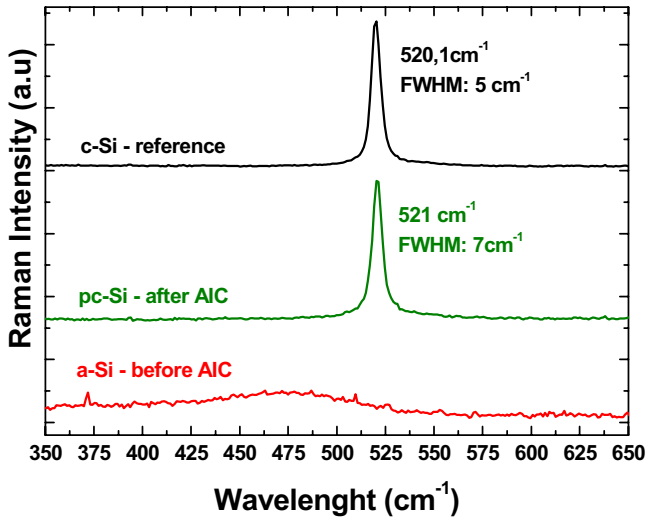

Fig. 3. Raman spectra of a representative sample (S3) before and after AIC annealing. A c-Si μ-Raman spectrum is also plot for reference purpose.

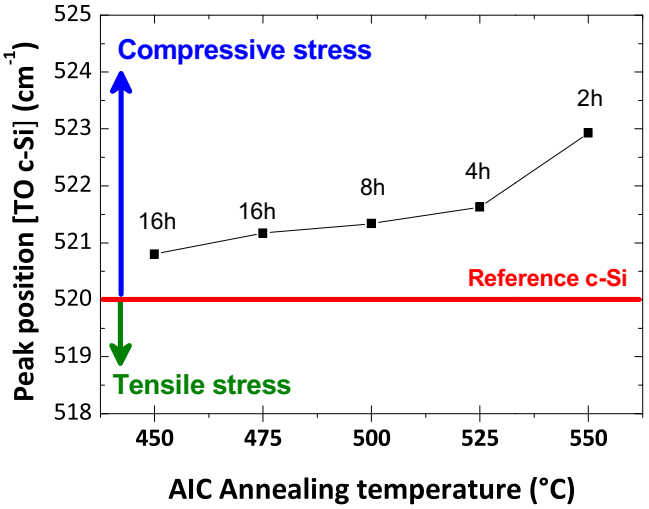

Fig. 4. Evolution of the Raman peak position as a function of the thermal treatment applied.

for sample S3 where F_c reaches 95%. A continuous pc-Si layer is formed for the following annealing conditions (525 °C – 4 h and 550 °C – 2 h).

3.2 Optical and structural analyses of the pc-Si layers

All the samples were analyzed by μ-Raman spectroscopy, before and after annealing. The system has been calibrated first with the transversal optic (TO) phonon band of a mono-crystalline silicon (c-Si) wafer. Representative spectra of the measurement is shown in Figure 3. The reference spectrum of the c-Si is also reported in the same graph for comparison.

Before AIC annealing, the amorphous phase of the as-deposited silicon is witnessed by a large band at around 480 cm^{-1}, attributed to the transverse optical (TO) phonons related band of a-Si [11]. After AIC annealing, a typical Lorentzian-like band centered at 521 cm^{-1} is attributed to the transverse optical (TO) band of crystalline silicon. On this spectrum, the band attributed to the amorphous silicon has totally disappeared which indicates the full crystallization of the pc-Si layer. The full half width maximum (FHWM) of the Raman peak is equal to 7 cm^{-1}, which is slightly higher than the 5 cm^{-1} of the c-Si reference. This value is similar for all samples, which means that the degree of crystallinity is relatively acceptable for all samples.

On the other hand, if we consider the Raman peak position versus the thermal budget as reported in Figure 4, we observe that the thermal budget has a considerable influence on the stress that affects the pc-Si layer.

Indeed, compressive stress induces a shift of the Raman peak to higher wavelengths. The correlation between the Raman shift and the stress can be roughly determined from the following formula [12]:

$$\sigma(\text{MPa}) = -250\,(\omega_s - \omega_0)$$

Table 2. Evaluation of the stress in the pc-Si layer according to the thermal treatment received.

Sample id.	Raman shift (cm^{-1})	σ (MPa)
S1	0.7	–175
S2	1.1	–275
S3	1.2	–300
S4	1.5	–375
S5	2.8	–700

where ω_0 is the wavenumber of the stressed free c-Si and ω_s is the wavenumber of the stressed pc-Si layer. The stress deduced value for each sample is reported in Table 2.

As the thermal treatment increases, the compressive stress observed in the layer is increasing too. A relative constant stress growth is observed from S1 to S4, from 175 up to 375 MPa respectively. For the sample S5, the stress is then raising strongly to reach 700 MPa. The stress in the layer can be induced by the grain boundaries which are known to compressively stress the pc-Si films [13]. The increase of the compressive stress is then correlated to the decrease of the grains size.

In order to investigate the crystallographic quality of the pc-Si layer more deeply, cross-sectional EBSD analyses were carried out. Prior to EBSD, a cross-sectional scanning electron microscopy observation of the sample was realized. This observation enables notably to check the surface quality of the polished surface. A picture of a representative sample is reported in Figure 5.

On this sample, the residual layer composed of aluminium and silicon islands on the top of the pc-Si surface has not yet been removed. The porous nature of this residual layer is clearly visible on this instructive picture. Thank to this cross sectional observation, each component of the multilayer can be clearly identified (metal/barrier layer/pc-Si/residual layer). Thus, the good quality of the layer exchange is clearly witnessed. The thickness of the pc-Si layer is about 200 nm, in accordance with the precursor aluminium layer's thickness.

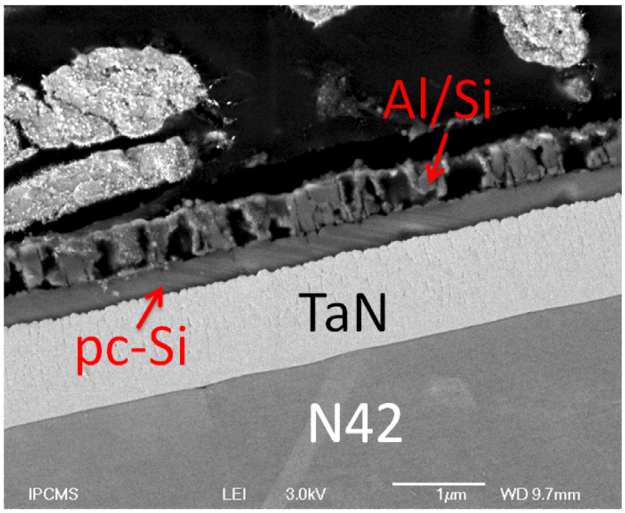

Fig. 5. Cross sectional scanning electron microscopy of a representative sample after AIC processing.

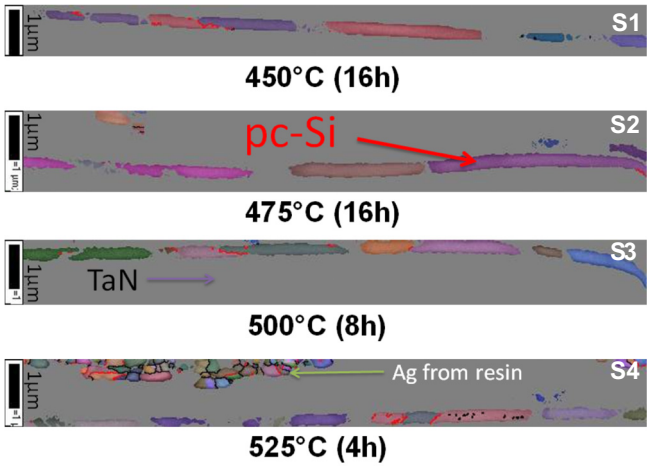

Fig. 6. Cross sectional orientation map deduced from EBSD observation (from top to bottom S1, S2, S3, S4 respectively). Each color in these images indicates a specific crystallographic direction.

The EBSD images of sample 1 to sample 4 are reported in Figure 6. Each color in these images indicates a specific crystallographic direction. The influence of the annealing conditions on the grain size can be therefore investigated. The portion of layers analyzed is too small to give reliable statistical values on the grain size; but it gives a good idea to define the optimization direction. Indeed, we can distinguish that the low annealing temperature results in much larger grain size (up to 5 μm for S1 and S2). This is clearly due to a lower nucleation rate at low temperature [14]. However, even if the grain size of the crystallites is higher, the pc-Si is not continuous for both of these samples, even though the longest annealing time of 16 h has been used. For S3, the pc-Si layer is not completely continuous (F_c = 95%), thus a longer time of annealing will certainly lead to a complete exchange of the layers. For S4, the apparent grain size is much smaller than for S3 but the layer is continuous (F_c = 99%).

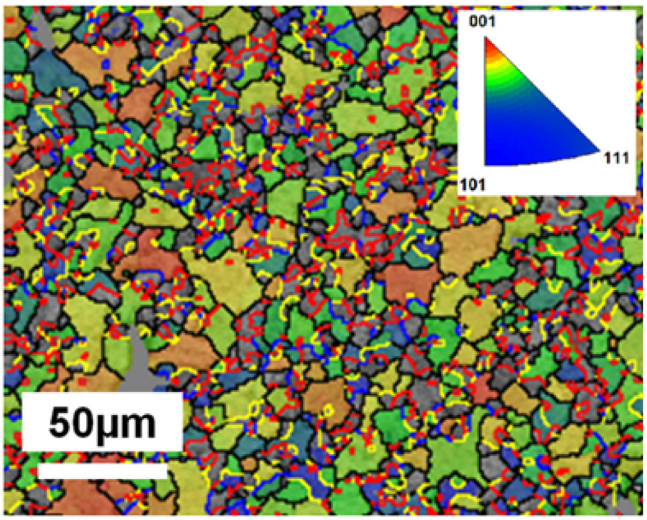

Fig. 7. Orientation map deduced from EBSD analysis. The lines shows the grain boundaries (twins: red = $\Sigma 3$, yellow = $\Sigma 9$, blue = $\Sigma 29$, black = randomly orientated). The inverse pole figure in the z-axis in reported on the inset (red color = high density, blue = low density).

As a summary, from the grain size estimation versus the exchange annealing conditions we can observe that the lowest the temperature conditions (S1 and S2) result in the biggest grains. However, the process is not completed after 16 h, which lead to non-continuous pc-Si layers. For the highest temperature conditions (S4 and S5), the pc-Si is continuous, but the grain size is limited to a few micrometers. In addition, the induced stress in the pc-Si is increasing with the temperature augmentation. Hence, the best compromise we choose to fit our requirements is to process the layer at 500 °C. At this temperature a consequent grain size is achievable. In order to complete the AIC process at this temperature the annealing time was increased up to 16 h.

4 Optimization results

Consequently to the previous experiments, a new sample was annealed at 500 °C during 16 h. After this process, the residual Al/Si layer was removed by chemical etching in order to achieve an EBSD plan view analysis. The plan view EBSD analysis is reported in Figure 7.

This observation is in good agreement with the expected optimization's results. Indeed, the EBSD orientation map shows a continuous pc-Si layer formed by AIC at 500 °C. The inverse figure pole reported in the inset Figure 6 indicates that there is preferential orientation along the ⟨100⟩ direction as usually reported for AIC layers [15]. From the orientation map, the grain size can be evaluated. For that purpose, a representative area of 1.44 mm^2 was analyzed. The extracted grain size distribution is reported in Figure 8.

The diameter of each grain is deduced by assuming disk geometry of a similar area. The grain size is comprised

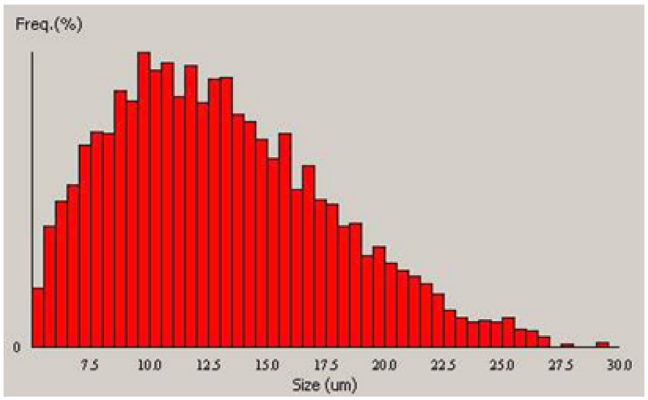

Fig. 8. Grain size distribution of the pc-Si thin films on metal substrate obtained by AIC after optimization.

between 3 to 30 μm with an average size around 15 μm. This result is, from our knowledge the best result obtained by AIC on metallic substrate up to now.

5 Conclusion

In this work, a-Si thin films were crystallized by AIC on a metallic substrate (Ni/Fe alloy) coated with a conductive diffusion barrier layer (TaN). The effects of the thermal budget on the pc-Si obtained were investigated in order to optimize the AIC process on such TaN coated metal substrates. The consecutive optical and structural analyses enabled us to achieve a continuous p-type pc-Si layer composed of the large grains ($\approx$15 μm on average) with limited residual stress. This work proves that a good crystallization can be obtained by AIC on metallic substrates (N42) coated with a TaN conductive barrier layer. The AIC method applied to metal substrate enables to produce pc-Si formed by larger grains than those achievable by a thermal annealing of a-Si or by CVD direct deposition of pc-Si. This result is promising is for the fabrication of thin film solar cell on a metallic substrate by the epitaxial thickening of the seed layer thus obtained. The electronic quality of the AIC seed layer is under evaluation by employing it into a solar cell.

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