

# Passivation effects of atomic-layer-deposited aluminum oxide

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**Abstract** Atomic-layer-deposited (ALD) aluminum oxide ( $\text{Al}_2\text{O}_3$ ) has recently demonstrated an excellent surface passivation for both  $n$ - and  $p$ -type  $c$ -Si solar cells thanks to the presence of high negative fixed charges ( $Q_f \sim 10^{12} - 10^{13} \text{ cm}^{-2}$ ) in combination with a low density of interface states ( $D_{it}$ ). This paper investigates the passivation quality of thin (15 nm)  $\text{Al}_2\text{O}_3$  films deposited by two different techniques: plasma-enhanced atomic layer deposition (PE-ALD) and Thermal atomic layer deposition ( $T$ -ALD). Other dielectric materials taken into account for comparison include: thermally-grown silicon dioxide ( $\text{SiO}_2$ ) (20 nm),  $\text{SiO}_2$  (20 nm) deposited by plasma-enhanced chemical vapour deposition (PECVD) and hydrogenated amorphous silicon nitride ( $a\text{-SiN}_x\text{:H}$ ) (20 nm) also deposited by PECVD. With the above-mentioned dielectric layers, Metal Insulator Semiconductor (MIS) capacitors were fabricated for  $Q_f$  and  $D_{it}$  extraction through Capacitance-Voltage-Conductance ( $C$ - $V$ - $G$ ) measurements. In addition, lifetime measurements were carried out to evaluate the effective surface recombination velocity (SRV). The influence of extracted  $C$ - $V$ - $G$  parameters ( $Q_f, D_{it}$ ) on the injection dependent lifetime measurements  $\tau(\Delta n)$ , and the dominant passivation mechanism involved have been discussed. Furthermore we have also studied the influence of the  $\text{SiO}_2$  interfacial layer thickness between the  $\text{Al}_2\text{O}_3$  and silicon surface on the field-effect passivation mechanism. It is shown that the field effect passivation in accumulation mode is more predominant when compared to surface defect passivation.

## 1 Introduction

It is well known that the thermal silicon oxide ( $\text{SiO}_2$ ) is a very good surface passivation material for crystalline Si ( $c$ -Si). However, the formation of thermal  $\text{SiO}_2$  requires a high-temperature process ( $>1000 \text{ }^\circ\text{C}$ ) which does not only increase the processing cost, but may also degrade the quality of the silicon wafer. Therefore, passivation materials that can be deposited at low temperatures are required. Hydrogenated amorphous silicon nitride ( $a\text{-SiN}_x\text{:H}$ ) obtained by plasma-enhanced chemical vapour deposition (PECVD) is commonly used as front surface emitter passivation and anti-reflection coating (ARC) for both  $n$ - and  $p$ -type low-resistivity  $c$ -Si solar cells. This material can be deposited by PECVD at low temperatures i.e. less than  $300 \text{ }^\circ\text{C}$ . Surface passivation of  $c$ -Si solar cell with atomic layer deposited (ALD) aluminum oxide ( $\text{Al}_2\text{O}_3$ ) is a good candidate for both  $p$ - and  $n$ -type surfaces as well as highly-doped  $p$ -type emitters, due to its very high built-in negative fixed charge density ( $Q_f \sim 10^{12} - 10^{13} \text{ cm}^{-2}$ ), low interface state density ( $D_{it} \leq 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ ) and low surface recombination velocity (SRV  $\leq 5 \text{ cm s}^{-1}$ ). Best reported conditions were obtained by plasma-ALD process

with film thickness ranging from 5 to 30 nm at deposition temperatures between  $150 - 250 \text{ }^\circ\text{C}$  followed by an annealing step in nitrogen or forming gas atmosphere at  $400 \text{ }^\circ\text{C}$  on low-resistivity Si wafers [1–6].

To understand the involved surface passivation mechanism, Girisch et al. [7] introduced an extended Shockley-Read-Hall (SRH) formalism to model the surface recombination mechanism, which included the effects of band bending due to fixed insulator charges ( $Q_f$ ) and charged interface states ( $D_{it} = qN_{it}$ ) over the entire band gap. By assuming the case of single defect level at mid-gap, the surface recombination rate ( $U_s$ ) can be written as an energy independent quantity [3, 7–10].

$$U_s \cong \frac{n_s p_s}{S_p + S_n} \quad (1)$$

where:

- $n_s$  and  $p_s$  are the surface concentrations of electrons and holes respectively.
- $S_n, S_p$  are the surface recombination velocity parameters given by  $S_n = \sigma_n v_{th} N_{it}$ ,  $S_p = \sigma_p v_{th} N_{it}$ .
- $\sigma_n, \sigma_p$  cross-section of electrons and holes respectively.
- $v_{th}$  being the thermal velocity.

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From the above equation (1) one can estimate the surface recombination velocity (SRV) at a particular injection level given by the excess carrier density ( $\Delta n$ ).

$$\text{SRV} = \frac{U_s}{\Delta n}. \quad (2)$$

Surface recombination rate ( $U_s$ ), can be reduced by altering two fundamental mechanisms:

- (i) *Reducing the interface state densities  $D_{it}$  (i.e. Chemical passivation)*

The  $D_{it}$  is dependent on material and chemical processes used in the fabrication of the solar cell. For example its reduction can be realized by diffusing hydrogen into the silicon/dielectric interface to replace the dangling bond defects.

- (ii) *Reducing the surface concentration of minority carriers (i.e. Field-effect passivation)*

The surface recombination rate ( $U_s$ ) can be reduced by decreasing one of two carrier concentrations at the silicon surface typically, the minority carrier concentration. This can be achieved by the fixed charges existing in the dielectric layer. Specifically, these charges create a built-in electric field which shields the minority carrier to be recombined at the surface by driving the device into accumulation or inversion modes depending on the charge sign (positive or negative) and the chosen substrate type [3, 8].

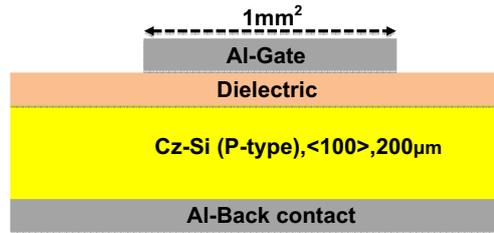
In this article we study the surface passivation mechanism induced by negative fixed charges in  $\text{Al}_2\text{O}_3$  films along with other fixed positive charge dielectrics. After a general introduction about the surface passivation mechanism, we describe the metal insulator semiconductor (MIS) capacitor device fabrication, lifetime sample preparations and electrical characterization techniques we used to extract the main parameters involved in the quality of the passivation, i.e.  $Q_f$ ,  $D_{it}$  and SRV in Section 2. Section 3 reports the experimental results of all the considered dielectrics. A discussion on the influence of films characteristics on the nature of interface passivation will be held. Subsequently, the impact of interfacial  $\text{SiO}_2$  layer on the field-effect passivation will be addressed in Section 4. Finally, in Section 5, conclusions are drawn from our  $\text{Al}_2\text{O}_3$  passivation study of Si surfaces.

## 2 Samples fabrication and characterization techniques

It clearly appears from equations (1)–(2) that insight knowledge about the density of interface states ( $D_{it}$ ) and surface concentrations of carrier  $n_s$ ,  $p_s$  (depends on  $Q_f$ ) gives in-depth information about the passivation quality of dielectric films. To extract these values we have considered MIS capacitors as test vehicle.

### 2.1 Dielectric film deposition

Thermal  $\text{SiO}_2$  was grown up to a thickness of 20 nm at 1050 °C in an ultra-dry oxygen atmosphere using vertical



**Fig. 1.** Schematic of the metal insulator semiconductor (MIS) capacitor.

furnace from Koyo Thermo Systems for a duration of 10 min.

For PECVD  $\text{SiO}_2$  20 nm-thick layers were deposited in a parallel plate reactor from Oxford Plasmalab system 100. The deposition parameters used during the film growth were: chamber pressure 0.8 Torr, deposition temperature 300 °C, gas flow:  $\text{SiH}_4$ -500 sccm,  $\text{N}_2\text{O}$ -20 sccm and  $\text{O}_2$ -5 sccm. PECVD a- $\text{SiN}_x$ :H 20 nm-thick layers were also deposited using the same Plasmalab system 100. In this case, Silane ( $\text{SiH}_4$ ) and ammonia ( $\text{NH}_3$ ) were used as reactive gases in the chamber. During the deposition,  $\text{SiH}_4$  was diluted to 5% in pure nitrogen. The deposition parameters used for the film growth were: chamber pressure 0.8 Torr, deposition temperature 300 °C, radio frequency (RF) power 20 W, plasma frequency 13.56 MHz, gas flow:  $\text{NH}_3$ -1.8 sccm,  $\text{SiH}_4$ -10 sccm, and  $\text{N}_2$ -700 sccm.

In the case of  $\text{Al}_2\text{O}_3$ , 15 nm-thick layers were deposited in a Fiji F200 ALD system from Cambridge NanoTech by thermal atomic layer deposition T-ALD and plasma enhanced atomic layer deposition PE-ALD. In both cases, trimethylaluminum precursor (TMA) from Sigma-Aldrich was used as aluminum source. Depositions were performed at 250 °C for both T-ALD and PE-ALD with argon as a carrier gas. Purge after precursor pulse is mandatory to avoid chemical vapor deposition. Before the deposition, all the samples were kept in the deposition chamber for 1800 s for pumping away  $\text{H}_2\text{O}$  or  $\text{O}_2$ . Each precursor flows separately through the deposition chamber. TMA pulse duration and purge time were 0.06 s and 10 s respectively for T-ALD and PE-ALD depositions. For T-ALD the precursor was de-ionized water while for PE-ALD, oxygen flow is used instead of water pulse. The flow was 30 sccm and plasma power was 300 W. The pulse duration and purge time of the plasma were 20 s and 5 s, respectively. The growth rates were observed to be 1 Å per cycle for both PE-ALD and T-ALD [11–15].

### 2.2 Device fabrication and C-V-G measurements

MIS capacitors were fabricated on p-type, Cz (100) silicon wafers with a resistivity of (1–3)  $\Omega$  cm as illustrated in (Fig. 1).

Before the deposition of the dielectric layers, all the wafers were cleaned using Piranha solution (3:1: $\text{H}_2\text{SO}_4$ : $\text{H}_2\text{O}_2$ , for a duration of 20 min at 120 °C). After the Piranha cleaning the wafers were dipped in dilute HF solution (1:50:HF:DI water) at room temperature

to remove the native oxide. The etching of native oxide layer is confirmed by the appearance of hydrophobic Si surface. Next, dielectric layers described in the above Section 2.1 were grown or deposited. Then, gate electrodes with an active area of  $1 \text{ mm}^2$  were patterned on the front side of the samples using an image reversal lithography step (i.e. resist coating, pre-bake, image exposure with mask, post-exposure bake, flood exposure and development). A 300 nm Al layer was evaporated on the front side of the samples followed by a lift-off in acetone. After front side device fabrication, full-area aluminum back contact (300 nm) is evaporated on the backside of the wafers. Finally, all the samples were annealed in forming gas ( $\text{N}_2/\text{H}_2$ : 90/10%) ambient at  $432 \text{ }^\circ\text{C}$  for 30 min.

Capacitance-voltage-conductance ( $C$ - $V$ - $G$ ) measurements were performed with Agilent B1500A Semiconductor device analyzer at different frequencies ranging from 1 kHz to 1 MHz. To confidently extract the interface trap charge densities ( $D_{it}$ ) at the silicon/dielectric interface we used different available extraction methods namely: High-Low frequency method, Terman method and Conductance method. The fixed charge density ( $Q_f$ ) in the dielectric was estimated from the flat-band voltage of the low-frequency  $C$ - $V$  curve [16–21].

### 2.3 Sample preparation for lifetime measurements

In our experiments, to emphasize the electronic properties of the dielectrics, we have chosen  $p$ -type, Boron doped,  $200 \text{ }\mu\text{m}$  thick double-side polished,  $\langle 111 \rangle$ , Float zone ( $FZ$ ) silicon wafers in order to neglect the bulk lifetime in SRV extractions. A choice of high resistivity  $>5000 \text{ }\Omega \text{ cm}$  wafers in particular is to avoid the band-gap defects induced by impurity dopants which acts like an effective recombination centers for SRH. Since the dopant impurity concentration sets the Fermi level, low-resistivity materials are more sensitive to these defects than high-resistivity material. So the dominant recombination in these samples is only due to Auger and radiative mechanisms. Lifetime measurements were performed using Sinton WCT-120 lifetime tester in both quasi steady state and transient modes. The different dielectric layers under consideration were symmetrically deposited on both sides of the wafers, followed by a forming gas annealing at  $432 \text{ }^\circ\text{C}$  for 30 min to activate the passivation mechanism [22, 23].

## 3 Passivation analysis using different dielectrics

The  $C$ - $V$  characteristics of MOS capacitors measured at 10 kHz for the different considered dielectrics are shown in Figure 2. The flat-band voltage ( $V_{fb}$ ) of the low-frequency  $C$ - $V$  curve allows calculation of the density and the polarity of charges present in the dielectric film from the following equation:

$$Q_f = (\Phi_{ms} - V_{fb})C_{oxide} \quad (3)$$

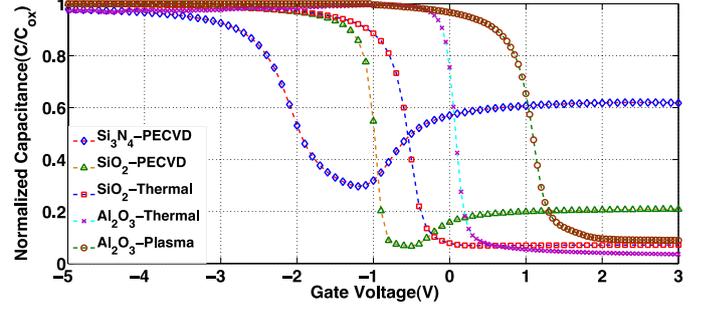


Fig. 2. Normalized  $C$ - $V$  Characteristics of different dielectrics at 10 kHz to extract the fixed charge density ( $Q_f$ ).

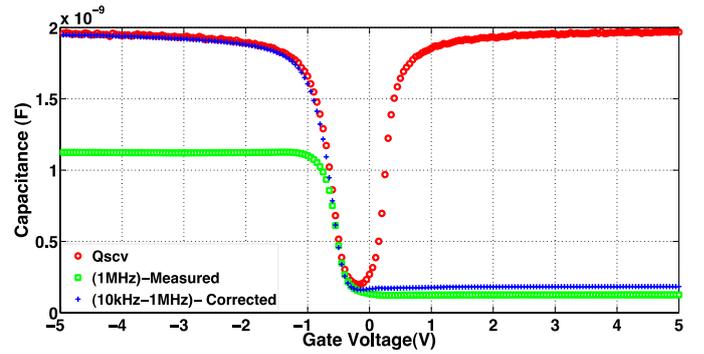


Fig. 3. Typical quasi-static (QSCV) and high-frequency (HF)  $C$ - $V$  curves for a MIS capacitor with  $\text{SiO}_2$  dielectric. The HF curve is also represented after parasitic free (frequency-dispersion related problems in accumulation gate voltages) correction using “dual-frequency five-element small-signal circuit model”.

where  $\Phi_{ms} = -0.96 \text{ V}$  is the difference between the aluminum and silicon work functions.

The flat-band voltage ( $V_{fb}$ ) of the MOS capacitors with the PECVD  $\text{Si}_3\text{N}_4$ , PECVD  $\text{SiO}_2$  and thermal  $\text{SiO}_2$  films is negative (i.e. lower than  $\Phi_{ms}$ ), meaning these films contain fixed positive charges ( $Q_f$ ). For the  $T$ -ALD and PE-ALD  $\text{Al}_2\text{O}_3$  films, the  $V_{fb}$  is positive and  $Q_f$  is negative [16–18].

### 3.1 Interface states densities ( $D_{it}$ ) extraction methodology

The extraction of interface state density ( $D_{it}$ ) using only one method may suffer from parasitic effects such as high leakage currents through the dielectrics (thin) films, series resistance from the measurement setup and frequency-dispersion related problems in accumulation region. These parasitic effects will definitively alter the measured capacitance-conductance ( $C$ - $G$ ) values, which will in turn affect the interpreted  $D_{it}$  by up to an order of magnitude. To minimize the influence of these effects on the extracted interface states densities ( $D_{it}$ ), all the measured  $C$ - $V$ - $G$  curves were first corrected for parasitic free  $C$ - $V$ - $G$  curves using “dual-frequency five-element small-signal circuit model” as shown in (Fig. 3) [19–21, 24].

To assure that the extracted  $D_{it}$  values are correctly estimated over the entire band gap and not affected by parasitic effects, we extract the  $D_{it}$  using three different methods described below.

Figure 4 exemplifies the measurement results for the MIS capacitor with PECVD  $\text{SiO}_2$  dielectric as an example using the different extraction methods as follows [16–21].

- Figure 4b shows the  $D_{it}$  extraction using high-low frequency method, which compares the quasi-static  $C-V$  (QSCV) curve with a high frequency (1 MHz)  $C-V$  curve. In the QSCV measurement the interface traps are assumed to follow the slowly varying dc bias, contributing to interface trap charge capacitance ( $C_{it}$ ). On the contrary, in the high-frequency  $C-V$  measurement the interface traps cannot follow the applied high-frequency ac signal, making the interface trap charge capacitance be zero ( $C_{it} = 0$ ). The value of  $C_{it}$  can then be estimated by comparing the difference in capacitance between quasi-static and high frequency  $C-V$  curves from depletion – inversion regions (i.e. yielding  $D_{it}$  for mid-gap potentials) [20, 21].
- Figure 4c illustrates the  $D_{it}$  extraction using Terman method, which is based on the stretch-out phenomenon in the experimental high-frequency  $C-V$  curve compared to theoretically simulated high-frequency  $C-V$  curve (i.e. ideal) with no interface traps. From the ideal  $C-V$  curve finding the surface potential ( $\varphi_s$ ) for a given capacitance value in the depletion regime, and interpolating it on the experimental gate voltage ( $V_G$ ) curve gives us the ( $\varphi_s - V_G$ ) relation. Repeating this for other points from accumulation to inversion regimes results in a ( $\varphi_s - V_G$ ) curve. This  $\varphi_s$  versus  $V_G$  curve is stretched-out when compared to theoretical curve without  $D_{it}$ , this stretch-out yields the information about the interface state densities [17, 19].
- Figure 4d represents the  $D_{it}$  extraction using conductance method. This method is based on measuring the equivalent parallel conductance per unit area ( $G_p$ ) as a function of bias voltage and frequency ( $\omega$ ). This equivalent parallel conductance represents the energy loss caused by capture and emission of carriers from the interface traps when gate bias is swept from accumulation to inversion regimes. Plotting ( $\frac{G_p}{\omega}$ ) with respect to frequencies in the depletion range of gate voltages yields the maximum of energy loss mechanism due to interface states. This peak (maximum energy loss) value of ( $\frac{G_p}{\omega}$ ) $_{max}$  gives direct information on  $D_{it}$  [16–18].

Tables 1 and 2 summarize extracted results from  $C-V$  measurements on MIS capacitors: oxide capacitance in accumulation ( $C_{ox}$ ), flat band voltage ( $V_{fb}$ ), fixed charge density ( $Q_f$ ) and interface trap charge density ( $D_{it}$ ) using different methods. The range of  $Q_f$  and  $D_{it}$  values are estimated considering variations of oxide thickness  $\pm(0.1-2)$  nm and substrate resistivity (1–3)  $\Omega$  cm.

Table 1 highlights that the PECVD  $\text{Si}_3\text{N}_4$  layer has a high density of positive charge  $\sim 4.2 \times 10^{12}$   $\text{cm}^{-2}$  compared to other dielectrics.  $\text{Al}_2\text{O}_3$  dielectric films exhibit

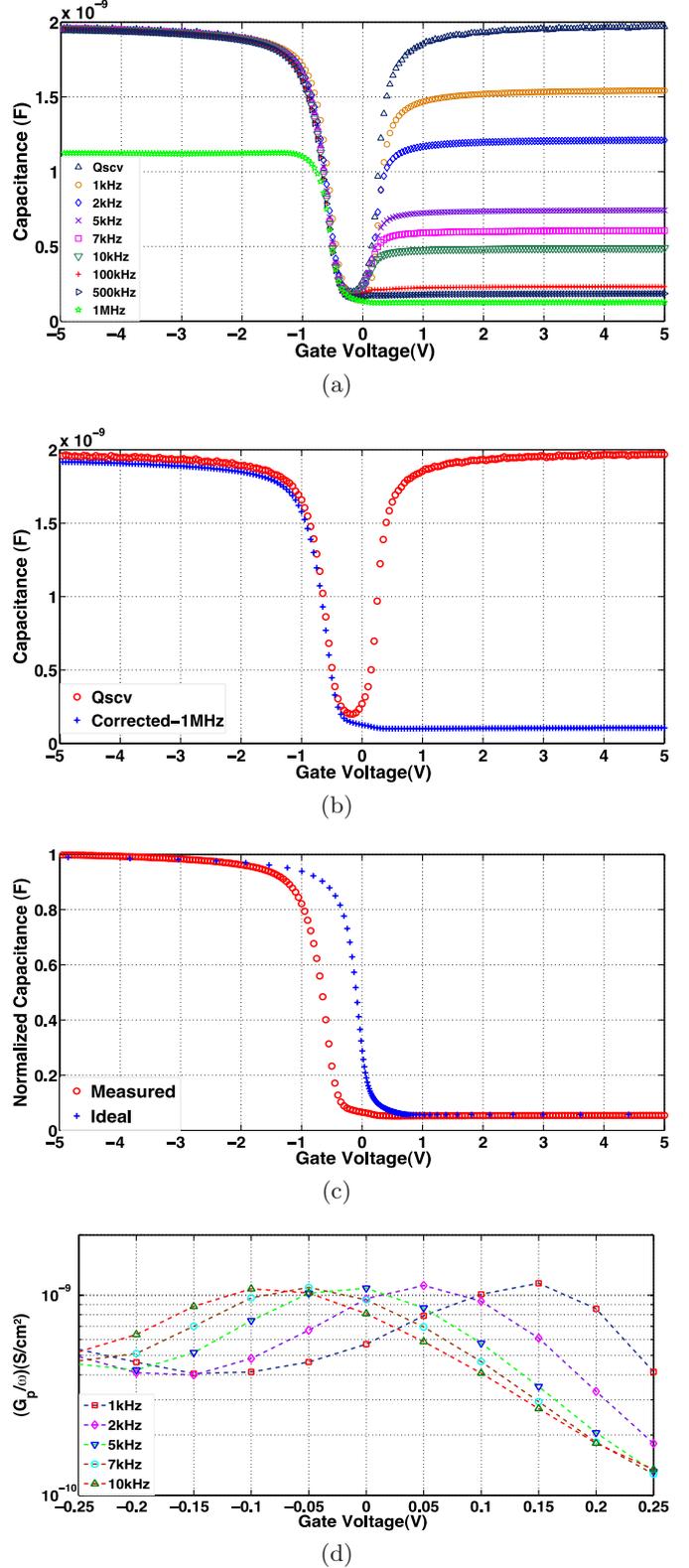


Fig. 4. PECVD-deposited  $\text{SiO}_2$  MOS Capacitor ( $C-V-G$ ) curves after parasitic effects correction using dual-frequency five-element circuit model: (a)  $C-V$  curves at different frequencies, (b)  $D_{it}$  extraction using high-low frequency method, (c)  $D_{it}$  extraction using Terman method, (d)  $D_{it}$  extraction using conductance method.

**Table 1.** Summary of extracted values for fixed charge density ( $Q_f$ ).

Dielectric layer	$C_{ox}$ (F/cm <sup>2</sup> )	$V_{fb}$ (V)	$Q_f$ (cm <sup>-2</sup> )	Literature reported $\sim Q_f$ (cm <sup>-2</sup> ) [3–5, 7–33, 35–42]
SiO <sub>2</sub> – Thermal (20 ± 1 nm)	$1.7 \times 10^{-7}$	-1.0	$+(3.3-4.7) \times 10^{10}$	$+(1-20) \times 10^{10}$
SiO <sub>2</sub> – PECVD (20 nm ± 2 nm)	$1.7 \times 10^{-7}$	-1.3	$+(2.3-3.9) \times 10^{11}$	$+(1-10) \times 10^{11}$
Si <sub>3</sub> N <sub>4</sub> – PECVD (20 nm ± 2 nm)	$3.0 \times 10^{-7}$	-3.0	$+(3.4-4.2) \times 10^{12}$	$+(4-80) \times 10^{11}$
Al <sub>2</sub> O <sub>3</sub> – Thermal (15 nm ± 0.1 nm)	$5.3 \times 10^{-7}$	-0.3	$-(2.1-2.3) \times 10^{12}$	$-(3-50) \times 10^{11}$
Al <sub>2</sub> O <sub>3</sub> – Plasma (15 nm ± 0.1 nm)	$5.3 \times 10^{-7}$	+0.6	$-(5.1-5.3) \times 10^{12}$	$-(2-13) \times 10^{12}$

**Table 2.** Extracted interface state density ( $D_{it}$ ) from  $C$ - $V$  measurements.

Dielectric layer	$D_{it}$ (cm <sup>-2</sup> eV <sup>-1</sup> ) (HF-LF method)	$D_{it}$ (cm <sup>-2</sup> eV <sup>-1</sup> ) (Terman method)	$D_{it}$ (cm <sup>-2</sup> eV <sup>-1</sup> ) (Conductance method)	Literature reported values [3–5, 7–33, 35–42]
SiO <sub>2</sub> – Thermal (20 ± 1 nm)	$(1.2-1.5) \times 10^{10}$	$(1.1-2.2) \times 10^{10}$	$(1.0-1.5) \times 10^{10}$	$(1-10) \times 10^{10}$
SiO <sub>2</sub> – PECVD (20 nm ± 2 nm)	$(2.5-2.9) \times 10^{10}$	$(2.3-3.5) \times 10^{10}$	$(2.2-3.2) \times 10^{10}$	$(5-30) \times 10^{10}$
Si <sub>3</sub> N <sub>4</sub> – PECVD (20 nm ± 2 nm)	$(1.3-1.7) \times 10^{11}$	$(1.6-2.7) \times 10^{11}$	$(1.3-2.4) \times 10^{11}$	$(5-50) \times 10^{10}$
Al <sub>2</sub> O <sub>3</sub> – Thermal (15 nm ± 0.1 nm)	$(1.1-1.2) \times 10^{11}$	$(1.0-1.6) \times 10^{11}$	$(1.9-2.3) \times 10^{11}$	$(6-10) \times 10^{10}$
Al <sub>2</sub> O <sub>3</sub> – Plasma (15 nm ± 0.1 nm)	$(1.6-1.8) \times 10^{11}$	$(1.7-2.1) \times 10^{11}$	$(2.9-3.3) \times 10^{11}$	$(8-20) \times 10^{10}$

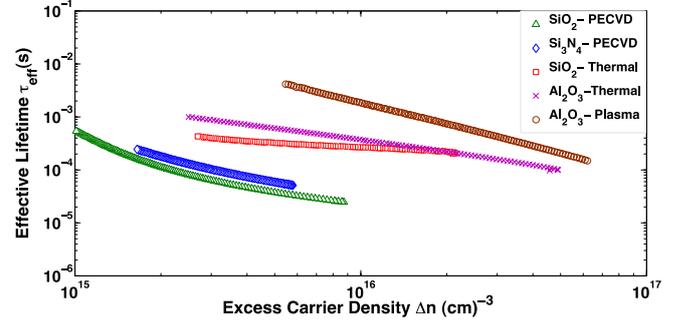
negative fixed charge densities as high as  $-5.3 \times 10^{12}$  cm<sup>-2</sup> and  $-2.3 \times 10^{12}$  cm<sup>-2</sup> when deposited by PE-ALD and  $T$ -ALD respectively. In our experiments, Al<sub>2</sub>O<sub>3</sub> deposited by PE-ALD exhibits more negative charges than  $T$ -ALD process. Table 2 summarizes the extracted  $D_{it}$  values using different methods. The relative differences can be related to the various specificities and sensitivity ranges of the different extraction methodologies, but also to the fact that the  $D_{it}$  values extracted from each method may not be extracted at the same gate voltage (i.e. depletion point). In addition, other errors could be due to non-uniform doping of the substrate, failure to obtain accurate 1 MHz high-frequency curves or inaccurate band bending during low-frequency measurements, which may affect the estimations. The  $D_{it}$  orders of magnitudes are correctly estimated and can be used as figures of merit to compare the different dielectrics. However, the  $D_{it}$  values extracted using conductance method on Al<sub>2</sub>O<sub>3</sub> PE-ALD,  $T$ -ALD samples exhibit slightly higher values due to the asymmetry of the capture cross-sections  $\sigma_n/\sigma_p$  in these dielectrics, influencing the extractions using this method [16, 25, 26].

### 3.2 Carrier lifetime measurements

To enable carrier lifetime testing, the respective dielectric layers were deposited on both sides of a wafer to maintain symmetrical structures. Supporting the above extracted  $C$ - $V$ - $G$  parameters ( $Q_f$ ,  $D_{it}$ ), minority carrier lifetime measurements (Fig. 5) show that thermally grown SiO<sub>2</sub> leads to a good passivation quality independent of injection level, mainly due to very low  $D_{it}$  [8, 9]. The quality of surface passivation is indeed also examined by effective surface recombination velocity ( $S_{eff}$ ) calculated from the lifetime measurements. A common typical injection point of  $\Delta n = 5 \times 10^{15}$  cm<sup>-3</sup> has been chosen for  $S_{eff}$  extraction for the comparison of the different dielectrics [8, 11, 12].

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + 2 \left( \frac{S_{eff}}{W} \right) \quad (4)$$

where  $W$  is the thickness of the substrate.


**Fig. 5.** Injection-level-dependent effective lifetime measurements on different dielectrics layers.

Assuming a very high lifetime, thanks to the use of  $FZ$  wafers equation (4) can be simplified and the maximum  $S_{eff,max}$  can be calculated by

$$S_{eff,max} \leq \left( \frac{W}{2\tau_{eff}} \right) \quad (5)$$

while the lower limit is the case where no recombination occurs. In reality the value of  $S$  lies in-between ( $0 < S < S_{eff,max}$ ) depending on the chosen injection level ( $\Delta n$ ) [8, 11, 12, 27, 28].

Table 3 presents the surface recombination velocities (SRV) extracted from the lifetime measurements using equation (5) for 200  $\mu$ m thick wafers covered with the different dielectrics. Samples with PE-ALD show the lowest SRV among all other dielectrics considered in this experiment with a value of less than 5 cm s<sup>-1</sup> though it presented the highest  $D_{it}$ .

Our experimental results have shown that a good silicon surface passivation is achieved with ALD Al<sub>2</sub>O<sub>3</sub> as dielectric film. This is attributed to a high density of negative fixed charges presented in the film, compensating the detrimental role of higher  $D_{it}$ .

The source of these negative fixed charges is attributed to the trapped hydroxyl groups in the film due to the deposition process [10, 14, 15, 29]. Another possible reason could be the presence of Al vacancies in the Al<sub>2</sub>O<sub>3</sub> film

**Table 3.** Extracted  $\tau_{eff}$ ,  $S_{eff,max}$  values from lifetime measurements at an injection point  $\Delta n = 5 \times 10^{15} \text{ cm}^{-3}$ .

Dielectric layer	$\tau_{eff}$ ( $\mu\text{s}$ ) at $\Delta n = 5 \times 10^{15}$	$S_{eff,max}$ ( $\text{cm s}^{-1}$ )	Literature reported $\sim S_{eff,max}$ ( $\text{cm s}^{-1}$ ) [3–5, 7–33, 35–42]
SiO <sub>2</sub> – Thermal (20 nm)	324	31	10–70
SiO <sub>2</sub> – PECVD (20 nm)	36	277	80–400
Si <sub>3</sub> N <sub>4</sub> – PECVD (20 nm)	56	178	30–1000
Al <sub>2</sub> O <sub>3</sub> – Thermal (15 nm)	613	17	5–30
Al <sub>2</sub> O <sub>3</sub> – Plasma (15 nm)	3790	3	2–20

or oxygen interstitials located at the Si/SiO<sub>x</sub>/Al<sub>2</sub>O<sub>3</sub> interfaces [3, 8, 9, 11, 12, 30]. Al<sub>2</sub>O<sub>3</sub> surface passivation can be described as a combination of both field-effect passivation and chemical passivation. Similar to other dielectrics, Al<sub>2</sub>O<sub>3</sub> also chemically passivates the surface by releasing hydrogen atoms, which diffuse to the Si/dielectric interface to passivate the dangling bond defects. Apart from this, Al<sub>2</sub>O<sub>3</sub> also serves the field-effect passivation mechanism due to its high fixed negative charge density, which is one-two orders of magnitude higher when compared to SiO<sub>2</sub> deposited by PECVD and two orders magnitude higher than thermally-grown SiO<sub>2</sub> (Tab. 1). This high amount of negative fixed charges in the overlying dielectric film drives the silicon surface into accumulation mode in case of *p*-type substrate creating a built-in *E*-field (electric field) at the surface shielding the minority carriers (here electrons) to recombine at the surface. This difference in field passivation significantly relaxes the requirements on the interface defect density ( $D_{it}$ ) at the c-Si/Al<sub>2</sub>O<sub>3</sub> interface. Figure 5 clearly shows two separate groups of curves, two lower curves corresponding to SiO<sub>2</sub>-PECVD and Si<sub>3</sub>N<sub>4</sub>-PECVD and three others. The field effect is more effective in the low injection regime, whereas at high injection, while photo-generated excess charges compensate the fixed charges that induced the field effect, and mainly the “chemical passivation” is dominant [3, 4, 8, 9, 11–13, 24, 30–33].

The shape of the  $\tau(\Delta n)$  curves (Fig. 5) can reveal information regarding the involved interface passivation mechanism [34].

- From Tables 1 and 2, PE-ALD and *T*-ALD Al<sub>2</sub>O<sub>3</sub> layers have almost same level of chemical passivation i.e. interface defect density  $D_{it} \sim (1-3) \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ . Thus the difference in lifetimes behavior especially at lower injection range can be solely attributed due to the field passivation. This is mainly induced by fixed charges in dielectrics. Comparing  $Q_f$  for the two Al<sub>2</sub>O<sub>3</sub> deposition processes, PE-ALD ( $Q_f \sim -5 \times 10^{12} \text{ cm}^{-2}$ ) is more efficient compared to *T*-ALD ( $Q_f \sim -2 \times 10^{12} \text{ cm}^{-2}$ ).
- PECVD-Si<sub>3</sub>N<sub>4</sub> layers exhibit poor chemical passivation ( $D_{it} \sim 2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ) in combination with a high density of positive  $Q_f \sim 4 \times 10^{12} \text{ cm}^{-2}$ . Even if the net charges is at the same level as Al<sub>2</sub>O<sub>3</sub>, the field effect passivation due to positively charged layers is less effective on *p*-type substrates resulting in a lower passivation quality. Accumulation mode caused by negative charges is more efficient than inversion caused by positive charges on *p*-type surfaces. This

difference is probably due to the depletion layer beneath the inversion layer where  $n_s$  and  $p_s$  concentrations are at the same level.

- Low fixed positive charges in PECVD-SiO<sub>2</sub> and thermal dielectric layers leads to weak inversion or depletion mode for which the resulting field effect is not efficient. SiO<sub>2</sub>-thermal lifetime curves exhibit almost injection independent behavior meaning that the dominant passivation mechanism involved at the interface is the chemical passivation, i.e. lowest  $D_{it} \sim 2 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ .

#### 4 Field effect passivation dependency on interfacial (SiO<sub>2</sub>) layer thickness

Kessels et al. [13] reported that a thin interfacial SiO<sub>2</sub> ( $\sim 1-2 \text{ nm}$ ) layer is formed naturally between Si surface and Al<sub>2</sub>O<sub>3</sub> layer. This thermal SiO<sub>2</sub> ( $\sim 1-2 \text{ nm}$ ) is the only means of chemical passivation at the interface. The thickness of this SiO<sub>2</sub> is too thin to completely passivate the interface states. Another disadvantage of this interfacial oxide is that it may not have the same quality as SiO<sub>2</sub> produced by thermal oxidation of Si. In some experiments we have introduced a stack of SiO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> on the Si surface. The main goal of this experiment is to chemically passivate the Si surface by thermally growing SiO<sub>2</sub> and maintains field-effect passivation with negative charges present in Al<sub>2</sub>O<sub>3</sub>. To perform this and investigate trade-offs between concurrent  $Q_f$  and  $D_{it}$  reductions, we have thermally-grown SiO<sub>2</sub> layers with two different thicknesses: 8 and 20 nm [11, 13].

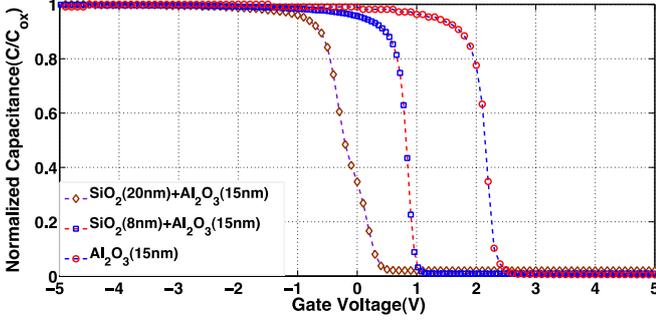
An Al<sub>2</sub>O<sub>3</sub> film of 15 nm was deposited on SiO<sub>2</sub> samples using PE-ALD. The deposition was also performed directly on the Si as a reference sample [3, 11–13, 24, 30–33]. All these samples were treated in the same way as in the earlier experiments for both *C-V-G* and lifetime measurements except that the Al<sub>2</sub>O<sub>3</sub> layer deposition was performed at 200 °C.

From SRV results, we observe that the SiO<sub>2</sub> (8 nm)/Al<sub>2</sub>O<sub>3</sub> (15 nm) stack exhibits the lowest SRV values compared to other samples. This can be correlated to negative  $Q_f$  and low  $D_{it}$  extracted (Tab. 4) from *C-V-G* curves (Fig. 6).

As reported by other authors [4, 13], the chemical passivation at the interface of Al<sub>2</sub>O<sub>3</sub>/Si occurs during the annealing step, when a very thin interfacial Al<sub>x</sub>SiO<sub>y</sub> layer is created in between the two materials. The formation of this layer is not well understood at this time as oxygen and hydrogen seem to play an important role,

**Table 4.** Parameters extraction on SiO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> stacks.

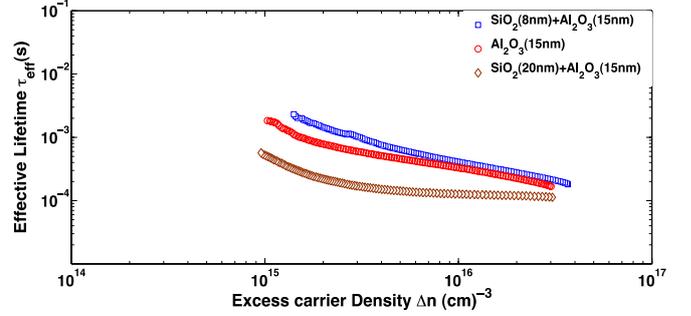
Stack type	$V_{fb}$ (V)	$Q_{fixed}$ (cm <sup>-2</sup> )	$D_{it}$ (cm <sup>-2</sup> eV <sup>-1</sup> ) (Terman method)	$\tau_{eff}$ ( $\mu$ s) @ $\Delta n = 2 \times 10^{15}$	$S_{eff, max}$ (cm s <sup>-1</sup> )
Al <sub>2</sub> O <sub>3</sub> (15 nm $\pm$ 0.1 nm)	1.6	$-(8.3-8.7) \times 10^{12}$	$(2.4-3.1) \times 10^{11}$	1110	9
SiO <sub>2</sub> (8 nm $\pm$ 1 nm) + Al <sub>2</sub> O <sub>3</sub> (15 nm $\pm$ 0.1 nm)	-0.65	$-(3.9-4.4) \times 10^{11}$	$(6.4-8.2) \times 10^{10}$	2320	4
SiO <sub>2</sub> (20 nm $\pm$ 1 nm) + Al <sub>2</sub> O <sub>3</sub> (15 nm $\pm$ 0.1 nm)	-0.1	$-(1.4-2.2) \times 10^{11}$	$(1.6-2.3) \times 10^{10}$	316	32


**Fig. 6.**  $C$ - $V$  characteristics of SiO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> stacks.

but consequences have been demonstrated and shown that electrically active interface traps were reduced. For the reference Al<sub>2</sub>O<sub>3</sub> sample, the flat-band ( $V_{fb}$ ) is positive and the density of negative fixed charges ( $Q_f \sim 8.5 \times 10^{12}$  cm<sup>-3</sup>) and the interface defect density ( $D_{it} \sim 2.7 \times 10^{11}$  eV<sup>-1</sup> cm<sup>-2</sup>) are higher than any other sample in this experiment. However, an SRV of 9 cm s<sup>-1</sup> is obtained from lifetime measurements meaning that the field effect passivation is predominant in this sample and slightly relaxes the requirement for lower  $D_{it}$  values.

For the sample with SiO<sub>2</sub> (8 nm)/Al<sub>2</sub>O<sub>3</sub> (15 nm) stack, the  $V_{fb}$  is negative but still exhibits negative fixed charges, however, twenty times lower than in the reference sample (only Al<sub>2</sub>O<sub>3</sub>). It is important to notice that the  $D_{it}$  also reduces by four times due to the presence of thermal-SiO<sub>2</sub> layer, which reduces the defects at the interface and also the field induced by Al<sub>2</sub>O<sub>3</sub> layer. This reduction of the effective field when using an SiO<sub>2</sub> layer can be explained by the fact that the charge centroid is driven away from the silicon surface with increasing SiO<sub>2</sub> thickness, as well as by the contribution of fixed positive charges in SiO<sub>2</sub> layer resulting in overall reduction of net effective negative charge density. However, the trade-off between  $Q_f$  and  $D_{it}$  obtained in these conditions leads to a much better effective lifetime at all injection levels. The difference is larger at low injection level where the field effect is the more efficient showing that 8 nm-SiO<sub>2</sub> does not shield too much the Al<sub>2</sub>O<sub>3</sub> charges [3, 4, 8, 9, 11–13, 24, 27, 28, 30–33].

In the case of thicker SiO<sub>2</sub> layer (20 nm), the “chemical interface” between Si and SiO<sub>2</sub> is the same as thinner SiO<sub>2</sub> (8 nm) layer. We can observe from Figure 7 that the effective lifetime is affected over the complete range of injection level.  $C$ - $V$  measurements on this sample confirm that the silicon oxide layer has reduced the interface trap charge density ( $D_{it} \sim 2.1 \times 10^{10}$ ) and also the fixed charges den-


**Fig. 7.** Lifetime measurements on SiO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> stacks.

sity ( $Q_f \sim -1.9 \times 10^{11}$ ). The effective lifetime is even lower than with Al<sub>2</sub>O<sub>3</sub> layer alone and has returned to the values previously obtained for SiO<sub>2</sub> only, meaning that field-effect passivation has been completely lost and the only means of passivation is due to chemical-passivation [10].

## 5 Conclusion

Electronic properties ( $Q_f$ ,  $D_{it}$ ) of different dielectrics were extracted. In addition, parasitic  $C$ - $V$ - $G$  corrections were applied to accurately estimate the interface trap charge density. Extracted parameters were discussed and compared with lifetime measurements to understand the passivation mechanisms involved at the interface.

In case of the PE-ALD Al<sub>2</sub>O<sub>3</sub> layer, the extracted fixed charge density is negative and about  $-5.2 \times 10^{12}$  cm<sup>-2</sup>, which provides an effective field-effect passivation for impeding the surface recombination of minority carriers. Interface trap charge density  $D_{it}$  has been calculated and is found to be about  $3 \times 10^{11}$  cm<sup>-2</sup> eV<sup>-1</sup> as a mean value in the depletion gate voltage range. Such high negative fixed charge density resulted in surface recombination velocity less than 3 cm/s due to formation of accumulation regime at the silicon surface.

We have demonstrated the dependency of field-effect passivation on the thickness of SiO<sub>2</sub> interfacial layer. From the  $C$ - $V$ - $G$  parameter extractions and lifetime measurements we concluded that an optimal thickness of SiO<sub>2</sub> (here 8 nm) reduces the interface state densities while still maintaining field-effect passivation. Thick SiO<sub>2</sub> layer reduces the net negative charge effect in the overall dielectric and may lead to a loss of the field-effect passivation.

We have observed that accumulation mode leads to better passivation than inversion mode. In our experiments, high negative fixed charges dielectrics were less sensitive to interface trap defects and exhibits better

passivation behavior over all injection range. More generally, for all dielectrics, field-effect passivation mainly drives surface recombination at low injection, as chemical passivation is more predominant at higher level.

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## References

1. B. Hoex, Ph.D. thesis, Technische Universiteit Eindhoven, 2008
2. S. Dauwe, Ph.D. thesis, University of Hannover, 2004
3. G. Dingemans, W.M.M. Kessels, *J. Vac. Sci. Technol. A* **30** (2012)
4. G. Dingemans, W.M.M. Kessels, *ECS Trans.* **41**, 293 (2011)
5. B. Hoex, J. Schmidt, P. Pohl, M.C.M. van de Sanden, W.M.M. Kessels, *J. Appl. Phys.* **104**, 044903 (2008)
6. B. Hoex, M.C.M. van de Sanden, J. Schmidt, R. Brendel, W.M.M. Kessels, *Phys. Stat. Sol. RRL* **6**, 4 (2012)
7. R.B.M. Girisch, R.P. Mertens, R.F. De Keersmaecker, *IEEE Trans. Electron Devices* **35**, 203 (1988)
8. S. Rein, *Lifetime Spectroscopy: A Method of Defect Characterization in Silicon for Photovoltaic Applications* (Springer Series in Materials Science, 2008)
9. G. Dingemans et al., in *35th IEEE PVSC, Honolulu, Hawaii, 2010*
10. A.G. Aberle, S. Glunz, W. Warta, *J. Appl. Phys.* **71**, 4422 (1992)
11. B. Hoex, F.J.J. Peeters, M. Creatore, M.A. Blauw, W.M.M. Kessels, M.C.M. van de Sanden, *J. Vac. Sci. Technol. A* **24**, 1823 (2006)
12. B. Hoex, S.B.S. Heil, E. Langereis, M.C.M. van de Sanden, W.M.M. Kessels, *Appl. Phys. Lett.* **89**, 042112 (2006)
13. W.M.M. Kessels, J.A. van Delft, G. Dingemans, M.M. Mandoc, *Review on the Prospects for the Use of Al<sub>2</sub>O<sub>3</sub> for High-efficiency Solar cells*, Workshop (Dept. of Applied Physics, Eindhoven University of Technology (TU/e), The Netherlands)
14. J.E. Crowell, *J. Vac. Sci. Technol. A* **21**, S88 (2003)
15. R.S. Johnson, G. Luckovsky, I. Bauvmol, *J. Vac. Sci. Technol. A* **19**, 1353 (2001)
16. D.K. Schroder, *Semiconductor material and device characterization*, 3rd edn. (John Wiley & Sons Inc., Hoboken, 2006)
17. E.H. Nicollian, J.R. Brews, *MOS (Metal Oxide Semiconductor) physics and technology* (John Wiley & Sons, New York, 1982)
18. R.F. Pierret, *Semiconductor Device Fundamentals* (Addison Wesley Publication, 1996)
19. L.M. Terman, *Solid-State Electron.* **5**, 285 (1962)
20. C.N. Berglund, *IEEE Trans. Electron Devices* **13**, 701 (1966)
21. R. Castagné, A. Vapaille, *Surf. Sci.* **28**, 157 (1971)
22. D.L. Meier, J.M. Hwang, R.B. Campbell, *IEEE Trans. Electron Devices* **35** (1988)
23. M.J. Kerr, A. Cuevas, *J. Appl. Phys.* **91**, 2473 (2002)
24. W.H. Wu, B.Y. Tsui, *Electron Device Lett. IEEE* **27** (2006)
25. F. Werner, A. Cosceev, J. Schmidt, *Energy Procedia* **319**, 27 (2012)
26. R. Engel-Herbert, Y. Hwang, S. Stemmer, *J. Appl. Phys.* **108**, 124101 (2010)
27. J. Schmidt, A. Merkle, R. Brendel, B. Hoex, M.C.C. van der Sanden, W.M.M. Kessels, *Prog. Photovolt.: Res. Appl.* **16**, 461 (2008)
28. B. Hoex, J. Schmidt, R. Bock, P.P. Altermatt, M.C.M. van de Sanden, W.M.M. Kessels, *Appl. Phys. Lett.* **91**, 112107 (2007)
29. D. Hoogeland, K.B. Jinesh, F. Roozeboom, W.F.A. Besling, M.C.M. van de Sanden, W.M.M. Kessels, *J. Appl. Phys.* **106**, 114107 (2009)
30. S.W. Glunz, D. Biro, S. Rein, W. Warta, *J. Appl. Phys.* **86**, 683 (1999)
31. B. Hoex, J.J.H. Gielis, M.C.M. van de Sanden, W.M.M. Kessels, *J. Appl. Phys.* **104**, 113703 (2008)
32. S. Steingrube, *Recombination models for defects in silicon solar cells*, Ph.D. thesis, Leibniz Universität Hannover, 2011
33. X. Tang et al., *J. Vac. Sci. Technol. A* **30** (2012)
34. C. Leendertz, N. Mingirulli, T.F. Schulze, J.P. Kleider, B. Rech, L. Korte, *Appl. Phys. Lett.* **98**, 202108 (2011)
35. J. Schmidt, B. Veith, F. Werner, D. Zielke, V. Tiba, P. Poodt, F. Roozeboom, A. Li, A. Cuevas, R. Brendel, Industrially Relevant Al<sub>2</sub>O<sub>3</sub> Deposition Techniques For The Surface Passivation Of Si Solar Cells, in *Proceedings of the 25th European Photovoltaic Solar Energy Conference, Valencia, Spain, 2010*
36. A.G. Aberle, *Crystalline Silicon Solar Cells: Advanced Surface Passivation and Analysis of Crystalline Silicon Solar Cells* (Centre for Photovoltaic Engineering, University of New South Wales Sydney, Australia, 1999)
37. P. Saint-Cast et al., *Appl. Phys. Lett.* **95**, 151502 (2009)
38. T.-T. Li, A. Cuevas, *Phys. Stat. Sol. RRL* **3**, 160 (2009)
39. G. Dingemans et al., Firing Stability of Atomic Layer Deposited Al<sub>2</sub>O<sub>3</sub> for C-Si Surface Passivation, in *Proceedings of the 34th IEEE Photovoltaics Specialists Conference, Philadelphia, Pennsylvania, USA, 2009*
40. J. Schmidt, B. Veith, R. Brendel, *Phys. Stat. Sol. RRL* **3**, 287 (2009)
41. J. Benick, A. Richter, M. Hermle, S.W. Glunz, *Phys. Stat. Sol. RRL* **3**, 233 (2009)
42. R. Hezel, K. Jaeger, *J. Electrochem. Soc.* **136**, 518 (1989)
43. A.G. Aberle, *Prog. Photovolt.: Res. Appl.* **8**, 473 (2000)
44. G. Agostinelli, P. Vitanov, Z. Alexieva, A. Harizanova, H.F.W. Dekkers, S. De Wolf, G. Beaucarne, Surface Passivation of Silicon by Means of Negative Charge Dielectrics, in *Proceedings of the 19th European Photovoltaic Solar Energy Conference, Paris, France, 2004*, pp. 132–134
45. S.M. George, *Chem. Rev.* **110**, 111 (2010)

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