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A modelling study of the performance of conventional diffused P/N junction and heterojunction solar cells at different temperatures

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Abstract Conventional crystalline silicon (c-Si) diffused P/N junction solar cells remain the largest contributor to solar electricity. In order to retain a high efficiency and as well, reduce the cost of solar electricity, Sanyo has proposed the "heterojunction with intrinsic thin layer (HIT)" solar cells where the emitter and the back surface field layers are deposited using low temperature (<200 °C) plasma processes, thus reducing the thermal budget and allowing for thinner wafers. Since solar cells are used in extremes of climate, we felt that it would be interesting to study the behaviour of c-Si and HIT cells, based on both P- and N-type wafers at different temperatures. Our results indicate that in HIT cells the amorphous doped layers form a heterojunction on the c-Si substrate, with a large valence band discontinuity that acts as a barrier for hole collection, specially at low temperatures. It is the aim of this article to investigate the effect of this valence band offset on solar cell performance at different ambient temperatures.

1 Introduction

Amorphous-crystalline (a/c) silicon "heterojunction with intrinsic thin layer (HIT)" solar cells, proposed by Sanyo [1,2] offer a low cost alternative to standard crystalline silicon (c-Si) solar cells with diffused P/N junction and back surface field (BSF) layers. This is because in HIT cells the P/N junction and BSF layer formation steps take place at a relatively low temperature (∼200 °C) using hydrogenated amorphous (a-Si:H) or polymorphous (pm-Si:H) silicon deposition technology, whereas in conventional c-Si cells the wafer has to be raised to ∼800 °C for junction and BSF layer formation by diffusion. This means not only a lower thermal budget, but also cost reduction from thinner wafers in "HIT" cells, since at ∼200 °C, there is little danger of a thin (∼100 μm) c-Si wafer becoming brittle. At the same time Sanyo [3] has demonstrated that in HIT cells, the high stable conversion efficiencies, characteristic of conventional diffused P/N junction solar cells, can be retained (since the absorber layer remains c-Si) by passivating the defects on the surface of the c-Si wafer, using a thin intrinsic amorphous silicon layer. Moreover, HIT cells have a lower temperature coefficient of conversion efficiency than standard c-Si cells, making them all the more suitable for practical applications [4,5].

Solar cells are used in extremes of climates – in hot regions, where there is plenty of sunshine, as well as in remote mountainous and polar regions, or in space, where a stand-alone source of energy is indispensable. It would, therefore, be interesting to analyze the relative performances of standard c-Si and HIT cells, in particular their illuminated current density-voltage (J-V) characteristics at different ambient temperatures. In this article we have first used detailed electrical-optical modelling of the dark and illuminated J-V characteristics of HIT cells on both P- and N-type wafers, where the hydrogenated amorphous silicon (a-Si:H) layers are deposited by the plasma-enhanced chemical vapour deposition (PECVD) technique [6]; to extract parameters that characterize the individual high efficiency cells. The latter fact guarantees that the defect states on the surface of the c-Si wafer have been well-passivated resulting in state-of-the-art high efficiency HIT cells. These parameters are then used with suitable modifications to take into account temperature effects, to predict the behaviour of these cells between around 175 K and 330 K, vis-à-vis that of standard diffused P/N junction solar cells.

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2 Experiments

To fabricate the HIT solar cells, high quality CZ P-type (doping level $\sim 9 \times 10^{14}$ cm^{-3}) or N-type (doping level $\sim 2 \times 10^{15}$ cm^{-3}) c-Si substrates were used. Their main properties are as follows: $\langle 100 \rangle$ orientation, $\sim$14 Ω-cm resistivity, 300 μm thickness and 4-inch diameter. The wafers have flat (non-textured) surfaces. The emitter and the BSF layers were deposited in a capacitively coupled PECVD reactor operating at an RF of 13.56 MHz [6] and resulting in a heterojunction (HJ) at both ends of the c-Si wafer (double HIT structure). The crystalline silicon wafers were dipped into hydrofluoric acid and immediately put into the reactor, which was pumped down to a pressure below 10^{-6} mbar before deposition. On both sides of the N-type c-Si and on the emitter side of the P-type c-Si wafers, $\sim$3 nm thick intrinsic amorphous silicon layers were first deposited using conditions that result in hydrogenated polymorphous silicon (pm-Si:H), i.e., at a relatively high pressure in the range of 1200 mTorr and at 200 °C. This material provides excellent passivation of defects on the surface of the c-Si wafer [7]. The highly phosphorous-doped N-a-Si:H layer, that acts as the emitter ($\sim$8 nm thick) on a P-type c-Si wafer; or as the BSF layer (thickness $\sim$20 nm) on N-type c-Si wafer was deposited at 200 °C. The material has a band gap of 1.8 eV and an activation energy of 0.20 eV. On the other face of the wafers, in the same RF-PECVD reactor and at 150 °C, highly boron doped, $\sim$20 nm thick P$^+$-a-Si:H layers were deposited. On the emitter layer of these structures an indium tin oxide (ITO) layer between 85 nm and 110 nm thick was deposited in a DC-magnetron sputtering setup. Lastly front contact metallization (with silver) was performed using serigraphy followed by annealing at a temperature of $\sim$200 °C under high pressure. A 15 nm aluminium layer was evaporated onto the BSF layer and annealed at a temperature of 150 °C to complete the back contact metallization. The structure of the cells was: for double HIT's on N-type substrate: ITO/ P-a-Si:H/ I-pm-Si:H/ N-c-Si/ I-pm-Si:H/ N^{++}-a-Si:H/ ITO/ Al; and for the double HIT's on P-type substrate: ITO/ N-a-Si:H/ I-pm-Si:H/ P-c-Si/ P^{++}-a-Si:H/ Al.

Basic solar cell parameters were obtained through current density-voltage (J-V) measurements under AM1.5 illumination. The complex refractive indices for each layer of the structure (that are required as input to the modelling program) have been measured by spectroscopic ellipsometry.

3 Simulation model

The "amorphous semiconductor device modelling program (ASDMP) [8,9]", later extended to also model crystalline silicon and HIT cells [10], solves the Poisson's equation and the two carrier continuity equations under steady state conditions for a given device structure, and yields the dark and illuminated J-V and QE characteristics. The gap state model consists of two monovalent donor-like and acceptor-like tail states and two monovalent Gaussian distribution functions (one being of donor type and the other of acceptor type) to simulate the deep dangling bond (DB) states, in the case of the amorphous layers (e.g. [11] (AMPS), [12] (AFORS-HET), [13]); while in the c-Si substrate, the tail states are absent. A more realistic gap state distribution model in a-Si:H would consist of, besides the monovalent band tail states, a deep defect distribution of DBs determined from the defect pool model (DPM) [14, 15]. However, in ASDMP, as in AMPS and AFORS-HET, since only monovalent states can be introduced, the deep DB distribution determined from DPM is replaced by two Gaussian distributions of monovalent states, donor like and acceptor like, separated by a correlation energy. Such a replacement has proved to be quite accurate in a-Si:H [16, 17].

The defect density on the surfaces of the c-Si wafer is modelled by a defective layer 3 nm thick. This means for e.g., that a surface defect density of 10^{11} cm^{-2} translates into a volume density of $\sim 3.3 \times 10^{17}$ cm^{-3}. Also the transport over the potential barriers at the contacts if any, is by thermionic emission and across the amorphous/ crystalline heterojunction by both thermionic emission and carrier diffusion. For example in P-a-Si:H/ N-c-Si HIT cells, holes are collected at the P-a-Si:H emitter end and, as will be seen later in Figure 3b, at this hetero-junction the valence band edge is closer to the Fermi level on the N-c-Si side than in P-a-Si:H, due to the valence band discontinuity, giving rise to a thin region on the N-c-Si side where the majority carriers are holes rather than electrons. This layer has been named the "inversion layer" [18], and, unless the defect density on the surface of the c-Si wafer is extremely high, the free hole density here is in fact higher than in P-a-Si:H, resulting also in hole diffusion across this heterojunction.

The generation term has been calculated using a semi-empirical model [19] that has been integrated into ASDMP [20]. Light enters through the ITO/emitter "front contact" which is taken at $x = 0$. Voltage is also applied here. The amorphous BSF / Al "rear contact" at the back of the c-Si wafer is taken at $x = L$, where L is the total thickness of the semiconductor layers; and is assumed to be at 0 V. For HIT cells on N-type wafers, the P-a-Si:H (emitter) / ITO front contact barrier height is 1.24 eV and the rear N-a-Si:H / Al contact barrier height =0.2 eV; while for HIT cells on P-type wafers, the rear P-a-Si:H (BSF) / Al contact barrier height is 1.20 eV and the front ITO / N-a-Si:H barrier height is 0.2 eV.

In our calculations we have taken into account the changes in the band gap, the effective densities of states at the conduction and valence band edges (N_c, N_v, respectively), carrier mobilities and dopant ionization as a function of temperature. We know that the band gap of c-Si decreases with increasing temperature approximately as [21]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta}, \tag{1}$$

where, $E_g(0)$ is the band gap of c-Si at 0 K, T is the absolute temperature, $\alpha = 4.9 \times 10^{-4}$ eV K^{-1} and $\beta = 655$ K.

Also the effective density of states (DOS) at the conduction and valence bands edges (N_c, N_v, respectively) decrease with decreasing temperature, following the 3/2 power law [22]. On the other hand, at a given doping density, the mobilities increase with decreasing temperature [22] as $T^{-2.42}$ in N-type c-Si and as $T^{-2.20}$ in P-type c-Si wafer.

For the case of a-Si:H, the variation of the band gap with temperature ia taken as:

$$E_g(T) = E_g(0) - 2.25 \times 10^{-4} T, \tag{2}$$

where $E_g(T)$ and $E_g(0)$ are the band gaps of a-Si:H at the given ambient temperature and at 0 K, respectively [13,23]. Obviously therefore the band offsets would be temperature dependent via the above variations of band gaps of c-Si and and a-Si:H with temperature; as well as of their electron affinities. However, we were unable to find any reference in the literature to determine whether the conduction band or the valence band moves with temperature, in other words the variation of the electron affinity with temperature is not known. We arbitrarily chose to hold the electron affinity of both c-Si and a-Si:H constant with temperature. This appears to be a crucial point, since as will be shown later, the deterioration of the performance of N-type HIT cells at low temperatures is primarily linked to the ΔE_v at the amorphous emitter/c-Si interface. In order to understand how important an exact determination of the a/c band offset at a given temperature is for determining HIT cell performance, we also performed some other simulations where we held not only the electron affinities of c-Si and a-Si:H constant with temperature, but also the band gap of a-Si:H. We found that the trend of deteriorating performance of HIT cells at low temperatures remains unchanged in both the above cases, leading us to believe that it is rather the transport mechanism of carriers across this barrier at low temperatures that plays a more vital role in determining HIT cell performance, rather than the exact value of ΔE_v as a function of temperature. In our calculations, we have assumed the same variation of the mobility in a-Si:H with temperature as has been assumed for c-Si above, while the effective DOS at the band edges in a-Si:H have been held constant with temperature. We suppose that these latter parameters, particularly in the doped a-Si:H layers would be less sensitive to temperature and have a small influence on HIT cell performance as a function of temperature. Also a more detailed modelling would require to consider the variation of TCO properties (e.g. barrier heights) on temperature. However, this would affect the simulation results of *both* standard P/N diffused junction and HIT cells and we suspect that the *relative* performance of these two types of cells (the primary aim of this study) would not be appreciably affected.

At room temperature and above we assume full ionization of the donor and acceptor impurity levels. However, we know that at lower temperatures, these levels are not fully ionized, and we calculate the density of the ionized donors and acceptors according to the formulae [22,24]:

$$\frac{N_D^+}{N_D} = \frac{\left\{\sqrt{8\frac{N_D}{N_C}\exp\left(\frac{E_D}{kT}\right)+1}\right\}-1}{4\frac{N_D}{N_C}\exp\left(\frac{E_D}{kT}\right)} \tag{3}$$

and

$$\frac{N_A^-}{N_A} = \frac{\left\{\sqrt{16\frac{N_A}{N_V}\exp\left(\frac{E_A}{kT}\right)+1}\right\}-1}{8\frac{N_A}{N_V}\exp\left(\frac{E_A}{kT}\right)}, \tag{4}$$

where k is the Boltzmann constant, T the ambient temperature, N_D^+ and N_A^- are the density of the ionized donors and acceptors, respectively; and N_D, N_A the total density of the donor and acceptor impurity atoms respectively; E_D, E_A the ionization energies of the donor (phosphorous) and acceptor (boron) impurity levels, respectively, taken equal to 0.044 eV and 0.045 eV [22].

4 Simulation of experimental results

We had in previous articles [25,26] simulated the illuminated J-V and quantum efficiency (QE) characteristics of HIT solar cells on P-type wafers, with amorphous emitter and BSF layers (double HIT structure) deposited by PECVD [6]. From these simulations we had extracted the parameters characterizing these solar cells, which we will utilize in the course of this article to predict the low temperature behaviour of these cells.

In this article, we simulate the dark and illuminated J-V characteristics of double HIT solar cells on N-type c-Si wafer, whose amorphous layers have been deposited under identical conditions (described in Sect. 2) and in the same PEVCD reactor [6]. We have simulated a series of HIT cells having different thickness of the intrinsic pm-Si:H layer covering that surface of the N-c-Si wafer that faces the P-a-Si:H emitter and the impinging light. Table 1 compares the measured solar cell output parameters under AM1.5 light, as well as the dark diode parameters, to the calculated values obtained using ASDMP. We find that in order to match experiments, lower values for the defect density (N_{ss}) on the surface of the c-Si wafer had to be assumed when this intrinsic layer was thicker. In a previous article, while modelling the extensive experimental results of Taguchi et al. [27], where the thickness of this intrinsic layer was varied, we had to make the same assumption, and had come to the conclusion that the main function of this intrinsic layer is to passivate the defects on the surface of the c-Si wafer on which it is deposited. This modelling result is consistent with the fact that in our deposition system [6], without load-lock, the defect density on the wafer surface decreases with increasing deposition time (film thickness) of the I-pm-Si:H buffer layer. It has been shown (e.g. [28]) that reduction of N_{ss} on that side of the N-type c-Si wafer facing the emitter layer, has a beneficial effect on both the open-circuit voltage (V_{oc}) and FF of the HIT cell – as is also observed in Table 1 (cases A to C). The surface defective layer (DL) is modelled by a ∼3 nm slice on the wafer surface. A similar

Table 1. Modelling of the experimental output parameters of HIT structure solar cells on N-type c-Si wafer at 300 K, having different thickness of the I-pm-Si:H layer on the emitter side (denoted by A, B, C, D). N_{ss} (DL) is the defect density on that surface of the c-Si wafer that faces the emitter. J_0 is the reverse saturation current density and n_0 the diode ideality factor calculated from the experimental and model generated dark J-V characteristics.

Cell name	I-pmSi:H thickness (nm)	N_{ss} (DL) (cm^{-2})		J_{sc} (mA cm^{-2})	V_{oc} (mV)	FF	Efficiency (%)	J_0 (mA cm^{-2})	n_0
A	2.5	9.2×10^{11}	Expt.	30.3	679	0.755	15.5	2.70×10^{-8}	1.30
			Model	31.2	673	0.758	15.9	2.41×10^{-8}	1.57
B	3.3	6.6×10^{11}	Expt.	30.8	683	0.767	16.1	1.60×10^{-7}	1.43
			Model	31.0	684	0.765	16.2	1.78×10^{-7}	1.77
C	4.0	4.5×10^{11}	Expt.	30.8	701	0.796	17.2	1.90×10^{-7}	1.49
			Model	31.1	701	0.807	17.6	1.10×10^{-7}	1.42
D	4.5	1.6×10^{11}	Expt.	30.6	706	0.732	15.8	5.90×10^{-8}	1.40
			Model	30.3	706	0.738	15.8	4.95×10^{-8}	1.67

Table 2. Measured parameters and those extracted by modelling deposited HIT cells on P-type [13–15] and N-type (present study) c-Si wafers. Note that the quantities marked with superscript "a" have been measured, those marked with superscript "b" have been taken from the literature, and those marked with superscript "c", supplied by the manufacturer. The defect density in the defective layer on the surface of the P-type c-Si wafer is 10^{11} cm^{-2} on the emitter side and 10^{12} cm^{-2} on the BSF side, while in the case of the N-type HIT cells these values are 4.5×10^{11} cm^{-2} and 10^{11} cm^{-2} at the emitter and BSF ends respectively, as extracted by modelling.

Parameters	P a-Si:H	I-pmSi:H (buffer)	N c-Si wafer	P c-Si wafer	N-a-Si:H
Layer thickness (μm)[a]	0.02	0.004	280	300	0.008–0.02
Mobility gap (eV)	1.75[a]	1.96[a]	1.12[b]	1.12[b]	1.8[a]
ΔE_v with respect to c-Si (eV)	–0.41	–0.46	0	0	–0.46
Donor (Accep) doping (cm^{-3})	(1.41×10^{19})[a]	0	2×10^{15}[c]	(9×10^{14})[c]	1.45×10^{19}[a]
Effective DOS in CB (cm^{-3})[b]	2×10^{20}	2×10^{20}	2.80×10^{19}	2.80×10^{19}	2×10^{20}
Effective DOS in VB (cm^{-3})[b]	2×10^{20}	2×10^{20}	1.04×10^{19}	1.04×10^{19}	2×10^{20}
Charac. energy (VB tail) (eV)[b]	0.05	0.05	–	–	0.05
Charac. energy (CB tail) (eV)[b]	0.03	0.03	–	–	0.03
Expon. tail prefact.(cm^{-3} eV^{-1})[b]	$4. \times 10^{21}$	$4. \times 10^{21}$	–	–	4×10^{21}
Elec. (hole) mobility (cm^2/V s)	25 (5)	25 (5)	1500 (500)[b]	1000(450)[b]	20 (4)
Gaussian defect density (cm^{-3})	8×10^{18}[a]	10^{15}	10^{12}	10^{12}	9×10^{18}[a]
Neutral σ (tails, midgap cm^2)	10^{-17}	10^{-17}	4×10^{-18}	4×10^{-19}	10^{-17}
Charged σ (tails, midgap cm^2)	10^{-16}	10^{-15}	4×10^{-17}	4×10^{-18}	10^{-16}

DL is assumed to exist at the rear side of c-Si facing the amorphous BSF; however, in previous simulations of HIT cells on N-type wafers [28], we had noted that the defect density here has less influence on device performance and had also explained why. We note that for case D with the thickest I-pm-Si:H layer, the fill factor (FF) and conversion efficiency deteriorate, in spite of a lower defect density (N_{ss}) on the N-c-Si surface. This is due to the fact that in these structures it is the I-pm-Si:H layer that is most resistive; therefore, when this layer is too thick, the FF falls. The short-circuit current density (J_{sc}) is relatively low in all cases as these cells have flat interfaces and no light-trapping schemes have been attempted.

The parameters for double HIT cells on P-type wafers, simulated by modelling their illuminated J-V and QE characteristics and given in references [25, 26], as well as those extracted by modelling the double N-HIT cells above, are summarized in Table 2. Of course the parameters marked by superscript "a" in Table 2, such as the thickness of the individual layers, the band gap, the doping and defect densities inside the emitter and BSF (deduced from measured activation energies), have been measured. Parameters, marked by superscript "b" in Table 2, have been taken from the literature, while the doping density in the N- and P-type c-Si wafers (marked by superscript "c") have been supplied by the manufacturer. The main parameters extracted by fitting the measured dark and illuminated J-V characteristics, therefore, are the defect densities on the surfaces of the c-Si wafers, their charged and neutral capture cross-sections and carrier mobilities inside the amorphous layers. It is relevant here to point out that in this article we are interested in evaluating the relative performances of various types of HIT cells at different ambient temperatures and comparing the results to the performance of standard P/N diffused homo-junction c-Si cells. Therefore, we chose for comparison, HIT cells

on N-type wafers whose amorphous layers were deposited in the same PECVD reactor [6] and under identical conditions as for HIT cells on P-type wafers simulated in references [25,26]. Unfortunately relatively little experimental results are available for this group of HIT cells on N-type wafers. Therefore, in our present simulations we had to depend heavily on our experience of simulating the extensive experimental results of HIT cells on N-type wafers produced by Taguchi et al. [27] and modelled in reference [28], and the interested reader is referred to these detailed simulations to get an insight and explanation of how the above parameters are extracted.

It maybe noted that we were unable to simulate all the above experimental results using the same values of the electron and hole mobilities in the emitter and the I-pm-Si:H layer sandwiched between it and the N-type c-Si wafer, as was also our experience in simulating the experimental results [27] in reference [28]. The electron and hole mobilities (μ_n, μ_p) in cases A, B were 7 cm^2/V s and 1.4 cm^2/V s, respectively, while for case D it was marginally lower (6 cm^2/V s and 1.2 cm^2/V s, respectively). However, a much higher value of these mobilities had to be assumed to simulate case C (25 cm^2/V s and 5 cm^2/V s, respectively). Increase of hole mobility over this region improves hole collection at the ITO/ P-a-Si:H interface and brings up the FF. In fact the high value of the FF and the conversion efficiency for case C may be assigned to higher carrier mobilities in the front amorphous layers, as well as reduced N_{ss}. The outstanding defect passivation properties of pm-Si:H has already been documented [7]. We also know that it has a higher hole mobility than a-Si:H [29]. Therefore, its use as the thin intrinsic layer on the wafer surface facing the emitter should also have a beneficial influence on the FF of the cell. However, up to this stage, such a high FF could only be achieved for the cell with a 4 nm thick intrinsic pm-Si:H layer (Tab. 1).

5 Results and discussion

The parameters given in Table 2 will be used in this section to study the performance of HIT cells at different temperatures using ASDMP. Again since the aim of this article is to compare the performance of standard P/N diffused junction c-Si solar cells and HIT cells, we have for the former case considered an N-type c-Si wafer, with the same properties and doping density as those given in Table 2 for the N-type wafer. In such a homo-junction structure, where the P/N junction and BSF layers are formed by diffusion in a furnace raised to ∼800 °C, the P-c-Si emitter layer is assumed to have a thickness of 0.25 μm, with a doping density of 5×10^{18} cm^{-3}, and the heavily N-doped 1 μm thick BSF layer of a similar doping density. Moreover, the surface recombination speeds at the contacts (which form the boundary conditions for the continuity equations) have been assumed to be equal to the thermal velocity (10^7 cm/s) in c-Si P/N diffused junction as well as in HIT cells. However, we know that whereas low defect densities and low recombination speeds at the a/c interfaces are crucial for attaining a high V_{oc} in HIT cells [10,28] it is rather the low surface recombination speeds of the minority carriers at the contacts that help improve V_{oc} in standard P/N diffused junction c-Si cells. Since in this study these have been assumed equal to 10^7 cm/s, the V_{oc} of our P/N diffused junction cells are relatively low. In all these calculations, the variations of the band gap of c-Si and the a-Si:H layers, the effective DOS at the band edges of c-Si, the carrier mobilities of both c-Si and a-Si:H, as also the fact that at low temperatures not all dopant atoms are ionized, have been taken into account (see Sect. 3).

Figure 1 compares the illuminated J-V characteristics of (a) a double HIT cell on N-type c-Si, (b) a double HIT cell on P-type c-Si, (c) the standard diffused P/N junction c-Si cell and (d) a front HIT cell on P-type wafer (where only the emitter layer is a-Si:H) at different temperatures. Figure 2 gives the solar cell output parameters – (a) the short-circuit current density, (b) the open-circuit voltage, (c) the fill factor and (d) the conversion efficiency of these cases as a function of temperature. We have in a previous article [28] simulated the solar cell output parameters of HIT cells on N-type wafers developed by Sanyo [27] with varying thickness of the intrinsic a-Si:H layer deposited on the wafer and facing the P-a-Si:H emitter. That study carried out between 343 K and 283 K, shows similar variation with temperature as Figure 2. Comparing Figure 1a to Figure 1b, we find that the HIT cell on N-c-Si has a better low temperature performance than the HIT cell on P-c-Si, the latter already showing an S-shape at 300 K. From Figures 1 and 2, it is obvious that the performance of HIT cells, in particular J_{sc}, FF and the conversion efficiency deteriorate sharply at low temperatures, the front HIT cell on P-c-Si being the only exception to this rule. The reason for this will be explained subsequently. Only the V_{oc} continues to increase. As temperature decreases, carrier densities in the bands decrease. This, therefore, means lower carrier recombination, a lower dark reverse saturation current density (J_{D0}) and hence via the formula:

$$V_{oc} = (nkT/q) \ln \left[(J_{sc}/J_{D0}) + 1 \right], \tag{5}$$

a higher open-circuit voltage at lower temperatures. This approximate formula ignores series and shunt resistances, but in the case of a c-Si absorber, with its surfaces well passivated to ensure low surface defect density, this is more or less true, even for HIT cells, where the absorber layer remains c-Si. A similar temperature dependence of V_{oc} has been obtained experimentally by Taguchi et al. [27] and while simulating these results [28].

To understand the difference in behaviour of the rest of the output parameters, we must refer to the fundamental difference between the standard diffused P/N junction and the HIT cell. The former is a homo-junction, while in the HIT device (in this article when referring simply to "HIT" cells, we mean double "HIT" cells with heterojunctions at both emitter and BSF ends), the emitter, the BSF and the intrinsic passivating layers are a-Si:H or pm-Si:H, with a band gap considerably higher than c-Si. In PECVD deposited samples, as in the present study,

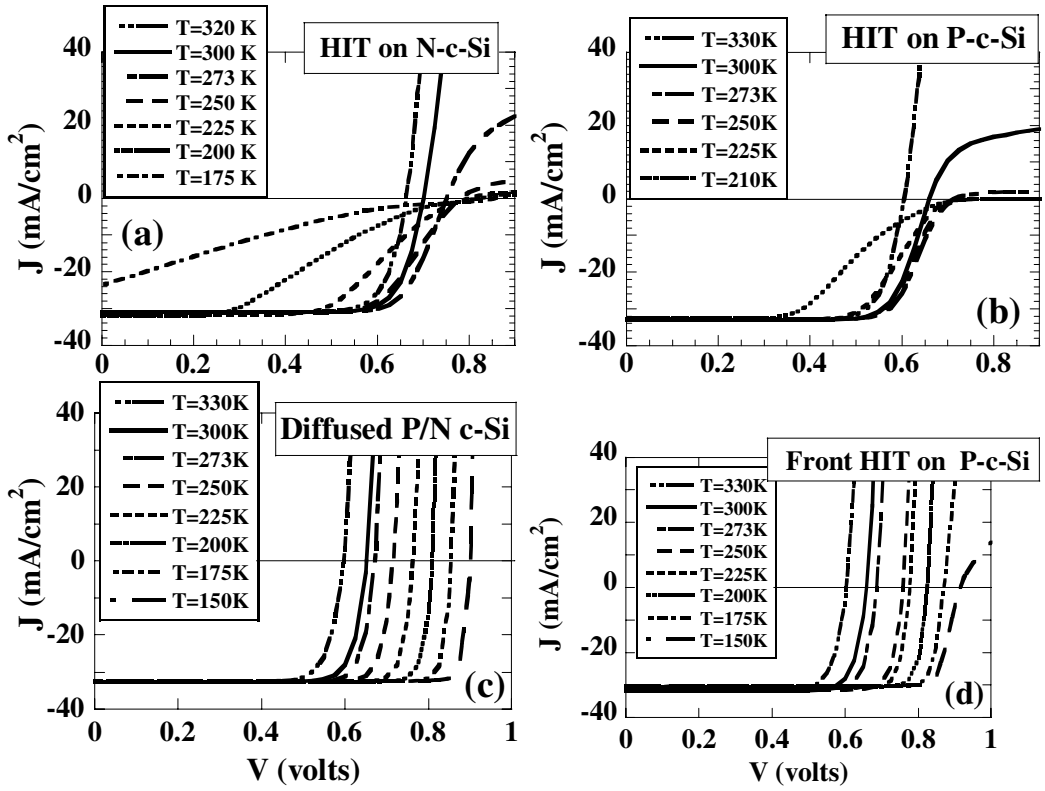

Fig. 1. Calculated illuminated J-V characteristics at various temperatures for different types of solar cells, all having c-Si as the absorber layer: (a) HIT cell on N-type wafer, (b) HIT cell on P-type wafer, (c) the conventional P/N diffused homo-junction solar cell and (d) front HIT cell on P-type wafer.

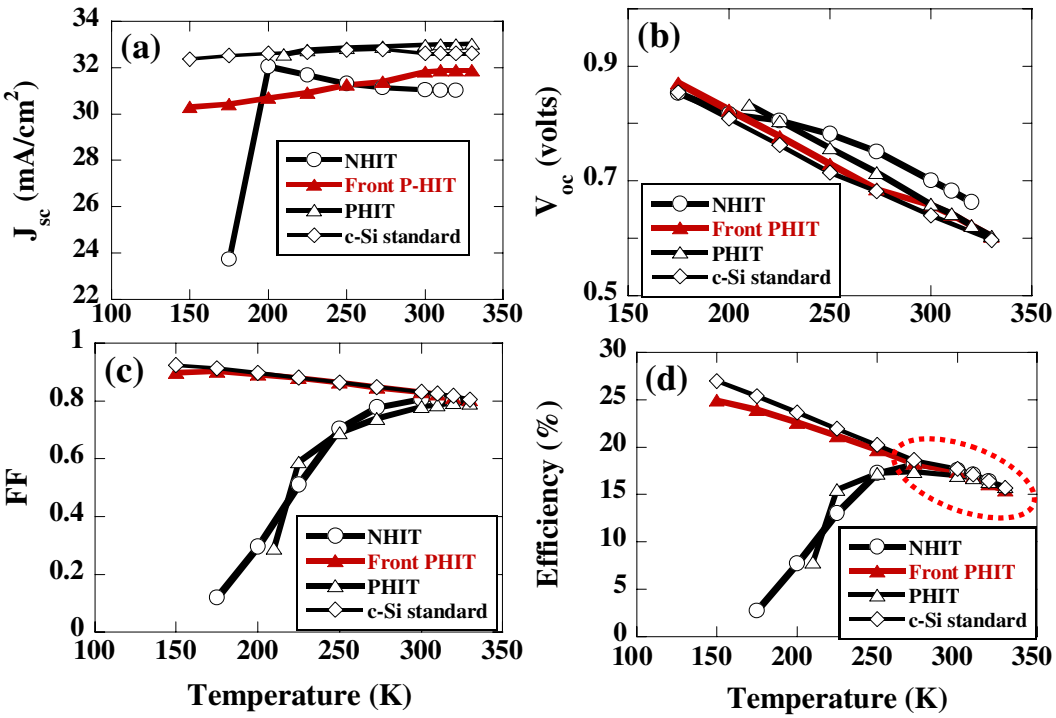

Fig. 2. Variation of the calculated values of (a) J_{sc}, (b) V_{oc}, (c) FF and (d) efficiency as a function of temperature for different types of solar cells having c-Si as the absorber. The lines are guides for the eye. The part encircled in red in (d) is expanded in Figure 5.

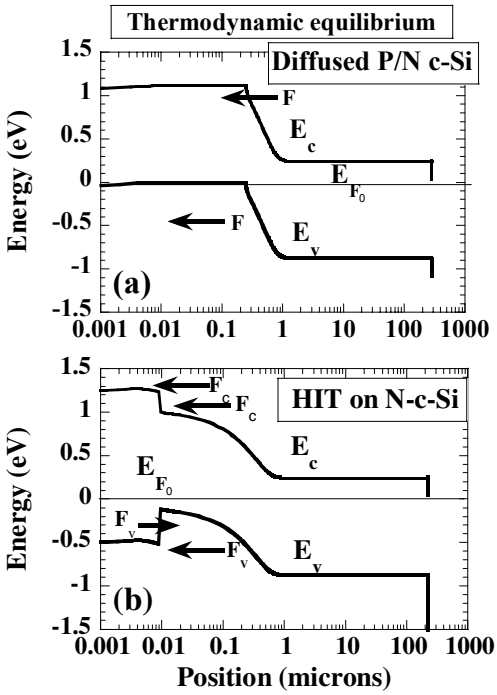

Fig. 3. Band diagrams in thermodynamic equilibrium at 300 K for (a) a conventional P emitter / N absorber homo-junction c-Si cell and (b) a HIT cell on N-type c-Si wafer. The directions of the electric field "F" on charge carriers in (a) and "F_c" on electrons and "F_v" on holes in (b) are indicated.

two-thirds of the band gap discontinuity falls on the valence band edge. In Figure 3, we draw the band diagrams of (a) the conventional P/N homo-junction cell, and (b) a HIT cell on N-type wafer at thermodynamic equilibrium, the main absorber layer in both cases being N-type c-Si with a P-type emitter. The directions of the electric field "F" on charge carriers in Figure 3a and "F_c" on electrons and "F_v" on holes in Figure 3b are indicated.

In these structures under illumination holes are collected at the top emitter side contact. But in the HIT structure, holes are faced with a barrier equal to the valence band discontinuity (ΔE$_v$) at the amorphous / crystalline HJ. At normal temperatures and provided ΔE_v is not too high [28], photo-generated holes can overcome this barrier by thermionic emission. There is also appreciable hole diffusion across this barrier unless the defect density at this a/c interface is extremely high, on account of the presence of an "inversion layer" on the N-c-Si side, as explained in Section 3. However, it has been shown [27,28] for P-a-Si:H/ N-c-Si HIT cells, that over the voltage range of interest in solar cell performance, tunnelling as means of hole transport is negligible and it is rather in the voltage range 0.1 V $< V <$ 0.4 V that this latter transport mechanism becomes important [27]. At low temperatures thermionic emission decreases, making it difficult for the photo-generated holes to surmount the ΔE_v potential barrier and resulting in S-shaped J-V characteristics (Fig. 1a) and a fall in FF, J_{sc} and efficiency (Figs. 2c, 2a, 2d) for the HIT cell. Similar results have been obtained by van Cleef et al. [30] in their study of P-a-SiC:H/ N-c-Si hetero-junction solar cells, where some tunnelling, probably multi-step tunnelling via the high defect density broad valence band tail of P-a-SiC:H has been reported. When the HIT cell is deposited on a P-type wafer, holes are collected on the rear BSF end, and then ΔE_v plays a similar role and hampers hole collection at the rear crystalline/ amorphous junction at low temperatures with similar effect on the illuminated J-V characteristics (Fig. 1b). The electrons, collected at the rear BSF end in HIT cells on N-type wafers and at the front emitter end in P-type HIT cells, face a much smaller barrier (ΔE_c), and moreover due to their higher mobility are easily collected and do not contribute to the S-shaped J-V characteristics of the HIT cells at low temperature.

For the case of the conventional diffused P/N homo-junction c-Si solar cell, whose band diagram is given in Figure 3a, there is no band discontinuity and, therefore, no potential barrier for carrier collection under illumination at any point of the device. Therefore, it retains good J-V characteristics (Fig. 1c) and a high value of the FF and efficiency, even at low temperature (Figs. 2c and 2d).

It is interesting to note that a front P-HIT cell (i.e., with a HJ at the emitter / P-c-Si junction only) retains good J-V characteristics for $T >$ 150 K (Fig. 1d). This is only to be expected as in P-HIT cells, holes are collected at the rear contact, where for this case there is no ΔE_v potential barrier. The N-a-Si:H / P-c-Si valence band discontinuity at the emitter end in all types of P-HIT cells is actually beneficial, pushing holes in the right direction, viz., towards the rear of the device. Thus, a front P-HIT cell would perform better at low temperatures compared to double HIT cells; however, this case is only of academic interest, since here the BSF layer needs to be formed by diffusion at high temperatures, thus compromising the advantages of the HIT configuration (low temperature process, therefore use of thinner wafers possible).

In Figure 4a, we plot the free hole density as a function of position inside the N-type HIT cell under light and short-circuit conditions at 300 K and 175 K. We find that at 175 K due to a reduction of the thermionic emission component, few holes can surmount the ΔE_v potential barrier, resulting in a pile-up of holes on the c-Si side of the device. Hole pile-up leads to a very strong electric field over a narrow region on either side of the amorphous / crystalline interface and a collapse of the electric field and flat bands over the rest of the depletion region inside c-Si (Fig. 4b), resulting in a sharp fall in the FF and the conversion efficiency (Figs. 2c and 2d) and ultimately also of J_{sc} (Fig. 2a). In fact, at 175 K, the strong accumulation of charge in c-Si can partially deplete even the highly defective P-layer, resulting in a shift of the depletion region from the c-Si side to the amorphous emitter layer (Fig. 4b). Again our results are similar to that of reference [30]. It is also interesting to note from Figure 4b that the ΔE_v potential barrier at 175 K has become extremely narrow, a condition that might favour tunnelling across this barrier. However, to the best knowledge of the authors, no report of such tunnelling across a

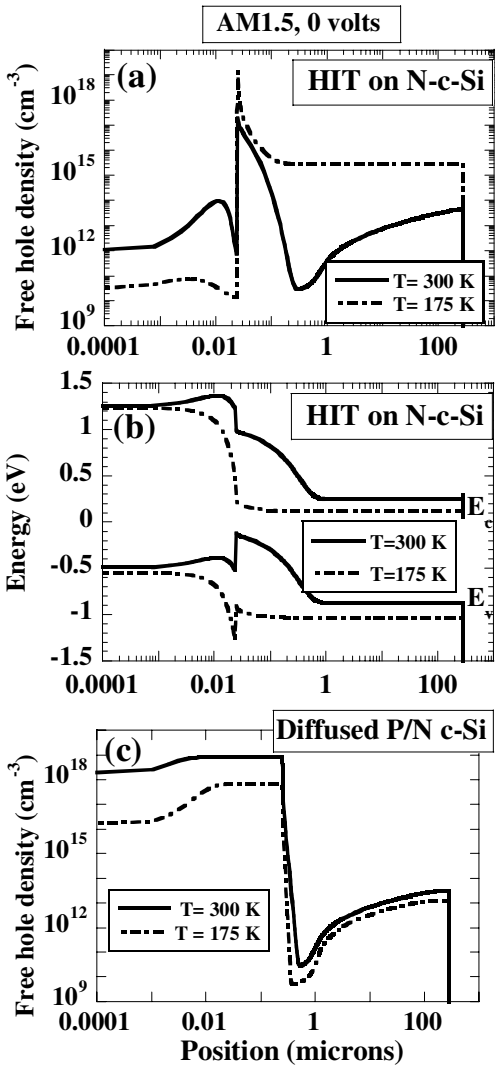

Fig. 4. (a) The free hole density as a function of position in the device and (b) the band diagram, under AM1.5 light and short-circuit conditions, for a HIT cell on N-type c-Si wafer at 300 K and 175 K, showing hole accumulation and virtual disappearance of the depletion region on the c-Si side of the amorphous-crystalline interface at 175 K; (c) the free hole density as a function of position under the same conditions and at the same temperatures for a standard P/N homo-junction c-Si solar cell.

P-a-Si:H / N-c-Si barrier under AM1.5 light has been reported. For comparison we plot the free hole density under illumination and short-circuit conditions for the standard c-Si homo-junction at 300 K and 175 K in Figure 4c and note that there is no charge accumulation in this case, leading to high values of FF (Fig. 2c) and efficiency (Fig. 2d) up to very low temperatures. In fact these parameters would have been even higher, but for the fact that we have taken account of partial donor and acceptor dopant ionization at low temperatures (Sect. 3). Only the current decreases slightly due to a fall in carrier concentration in the bands at low temperatures.

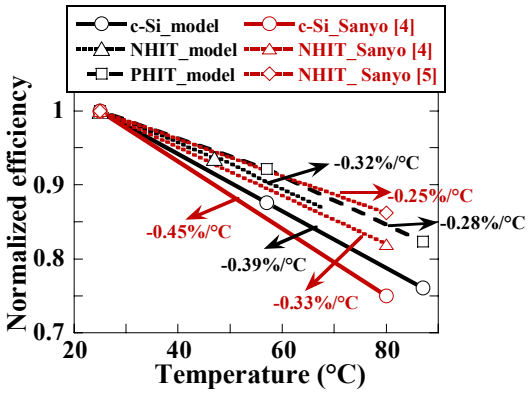

Fig. 5. Comparison of the normalized efficiency of solar cells of different structures obtained from our model with the published results of Sanyo [4,5]. The latter are shown in red, while our results are in black. The temperature coefficient of the normalized conversion efficiency for the conventional P/N diffused junction solar cell is –0.45% / °C (Sanyo [4]), while it is –0.39% / °C in our case. For HIT cells on N-type wafers, Sanyo results vary from –0.33% / °C [4] to –0.25% / °C [5], while it is –0.32% / °C in our case. For HIT cells on P-type wafers we obtain a temperature coefficient –0.28% / °C.

In Figure 5, we have zoomed in on that part of the conversion efficiency versus temperature curve, that is encircled in red (temperature range between 298 K and 330 K) and plotted the normalized efficiency versus temperature. Our curves are compared to the experimental results of Sanyo [4,5]. The temperature coefficient of the normalized conversion efficiency for the conventional P/N diffused junction solar cell is –0.45% / °C [4], while it is –0.39% / °C in our case. For HIT cells on N-type wafers, Sanyo results vary from –0.33% / °C [4] to –0.25% / °C [5], while it is –0.32% / °C in our case. For HIT cells on P-type wafers, we obtain a temperature coefficient –0.28% / °C. Thus both experiments and our modelling results indicate that HIT cells have a lower temperature coefficient of conversion efficiency than the conventional diffused P/N junction solar cell making them more suitable for use at high temperatures.

6 Conclusions

We have compared the performance of standard P/N diffused junction and HIT solar cells at different ambient temperatures. This has been done since, as mentioned in the introduction, solar cells are used in extremes of climate and therefore we need to know which type of solar cell is particularly suited for use under specific conditions. Our study clearly indicates that HIT cells are disadvantageous for use below 250 K, as their performance deteriorates sharply on account of the large amorphous-crystalline valence band discontinuity and reduced thermionic emission across this barrier at low temperatures. However, they are well-adapted for use in hot and sunny regions of the planet, not only because of their lower production cost, but also because they have a lower temperature coefficient of conversion efficiency compared to the standard diffused

P/N junction solar cell. However, as also demonstrated in this study, the latter class of cells is clearly better-suited for low temperature and space applications.

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