EPJ Photovoltaics **3**, 35005 (2012)
www.epj-pv.org
DOI: 10.1051/epjpv/2012009

Evolutionary process development towards next generation crystalline silicon solar cells: a semiconductor process toolbox application

J. John[1,a], V. Prajapati[1,2], B. Vermang[1,2], A. Lorenz[1,2], C. Allebe[1,2], A. Rothschild[2], L. Tous[2], A. Uruena[2], K. Baert[2], and J. Poortmans[2]

[1] IMEC, Kapeldreef 75, Leuven, Belgium
[2] Katholieke Universiteit Leuven, Leuven, Belgium

Received: 8 August 2011 / Accepted: 29 May 2012
Published online: 14 August 2012

Abstract Bulk crystalline Silicon solar cells are covering more than 85% of the world's roof top module installation in 2010. With a growth rate of over 30% in the last 10 years this technology remains the working horse of solar cell industry. The full Aluminum back-side field (Al BSF) technology has been developed in the 90's and provides a production learning curve on module price of constant 20% in average. The main reason for the decrease of module prices with increasing production capacity is due to the effect of up scaling industrial production. For further decreasing of the price per wattpeak silicon consumption has to be reduced and efficiency has to be improved. In this paper we describe a successive efficiency improving process development starting from the existing full Al BSF cell concept. We propose an evolutionary development includes all parts of the solar cell process: optical enhancement (texturing, polishing, anti-reflection coating), junction formation and contacting. Novel processes are benchmarked on industrial like baseline flows using high-efficiency cell concepts like i-PERC (Passivated Emitter and Rear Cell). While the full Al BSF crystalline silicon solar cell technology provides efficiencies of up to 18% (on cz-Si) in production, we are achieving up to 19.4% conversion efficiency for industrial fabricated, large area solar cells with copper based front side metallization and local Al BSF applying the semiconductor toolbox.

1 Introduction

The photovoltaics (PV) sector is a strongly growing industrial sector with a compound annual growth rate of 33% over the last 3 decades (Fig. 1). It is expected that this growth rate could remain up to 40%/year for this decade as a result of the efforts made worldwide to reduce dependence on fossil fuel and the CO_2-emissions related to electricity generation. Exemplary in this respect is the decision of the European Commission to go for a share of 20% renewable energy sources in 2020 in the European energy mix (with a share as high as 30% for electricity generation). As a result of this sustained growth, the photovoltaic sector which measures at this moment 25−30 billion $ (the value of the PV-systems market) in financial terms, will become a plus 100 billion $ sector in 2020.

The cost of Si material constitutes about 1/3 of the solar cell module cost [1]. In order to be less dependent on price fluctuations of polysilicon feedstock and wafers, and to eventually realize cost targets down to 0.5 euro/Wp, an evolution towards a reduction of "grams of pure Si/Wp" is taking place. As one does not want to sacrifice solar cell efficiency despite the use of thinner wafers, this requires quite drastic changes for crystalline Si solar cell technology. As a basic trend one could state that the objective is to reduce the grams of Silicon per Wp by a factor of 2 with an efficiency increase of roughly 20% relative (from 17−18% → >20% for industrial crystalline Si solar cells) [2].

2 Experimental results

2.1 Efficiency improvement potential: the toolbox application

The output efficiency of mono-crystalline Silicon solar cells in production is ∼17.5%. This is ∼12.5% less than predicted by theory taking the Auger Recombination limit into account. These losses can be specified in three main parts: electrical losses in the bulk and the surface due to SRH recombination processes, optical losses due to insufficient optical confinement of the cell and resistive losses on the contacts. Figure 3 depicts the distribution of the losses in mono-crystalline Silicon solar

[a] e-mail: joachim.john@imec.be

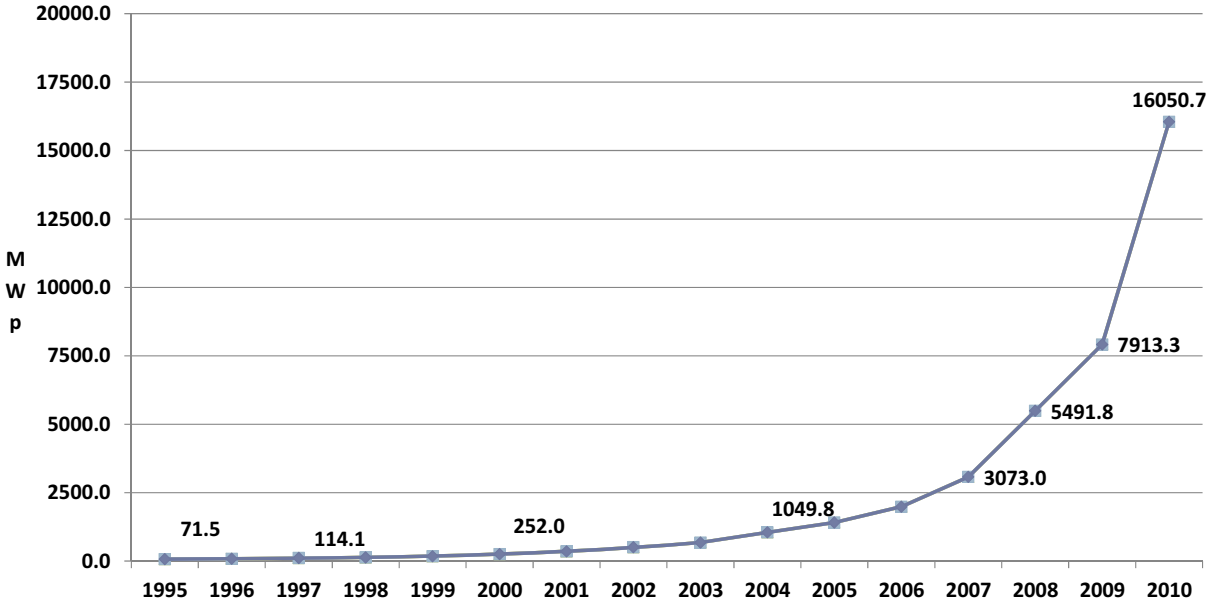

Fig. 1. PV Industry Growth 1995 to 2010 [source: Navigant consulting].

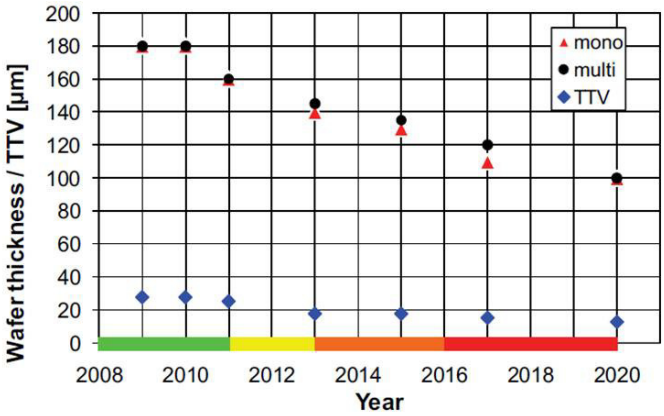

Fig. 2. Thickness development roadmap for crystalline silicon solar cells, wafer thickness and total thickness variation is depicted, the green code indicates that technical solutions are known, yellow means industrial solution is known but not yet in production. Orange means interim solution is known, too expensive or not suitable for production, whereas red means that no solutions for high-volume manufacturing of such thin wafers with high yield are available yet. [source: International Technology Roadmap for Photovoltaics (ITRPV.net). Results 2010] [2].

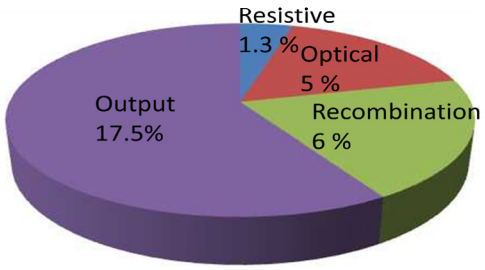

Fig. 3. Losses in monocrystalline cz-Si solar cells. Maximum efficiency = 29.8% (Auger limit), the recieved efficiency in production is ∼17.5%, losses due to recombination ∼6%, optical losses due to insufficient optical confinement ∼5% and 1.3% resistive losses at the contacts [3].

cells after MacDonalds [3]. To overcome the losses successive improvement of the different solar cell processes is required. The Passivated Emitter and Rear Locally diffused cell concept depicted in Figure 4 has a number of features added to overcome the losses present in the full Aluminum back-side field solar cell.

The semiconductor process toolbox is benchmarked in an industrial Passivated Emitter and Rear Locally diffused cell concept (i-PERL) on 148 cm^2, 150 um thick, (1−3 Ω cm) cz-Si material, as depicted in Figure 4.

In comparison to the full Al BSF cell, the following features are added:

- Fine line front metallization (reduce shadowing losses).
- Shallow or deep emitter (reduce recombination losses in the emitter, enhance blue responsivity).
- Dielectric rear passivation (reduce surface recombination losses).
- Laser ablated vias in rear passivation (reduce contacting recombination losses).
- Textured front side and polished rear side (enhance optical confinement, enhance infrared responsivity).
- Physical vapor deposition (PVD) of back-side metallization (reduce metal consumption, contactless processing, increase optical confinement, e-beam or sputtering of Al).

The SEMI PV road map predicts a decrease of the emitter saturation current below 100 fA/cm^2 in 2020 (Fig. 5). In order to reach this value the emitter formation process has to be optimized. The challenges are that higher ohmic emitters with lower surface concentration have to

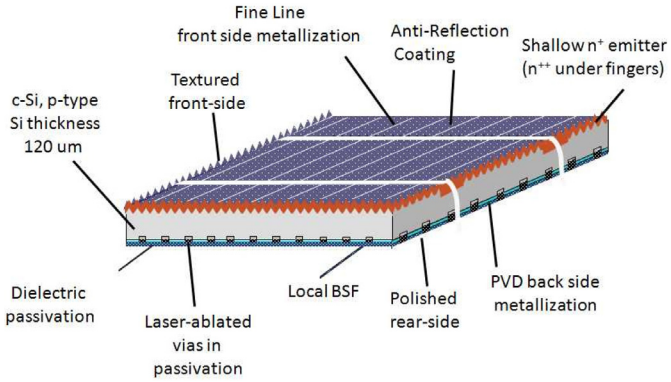

Fig. 4. Industrial Passivated Emitter and Rear Locally diffused cell concept (i-PERL), 120−150 um thick, 1−3 Ω cm, 156 cm^2, cz-Si material.

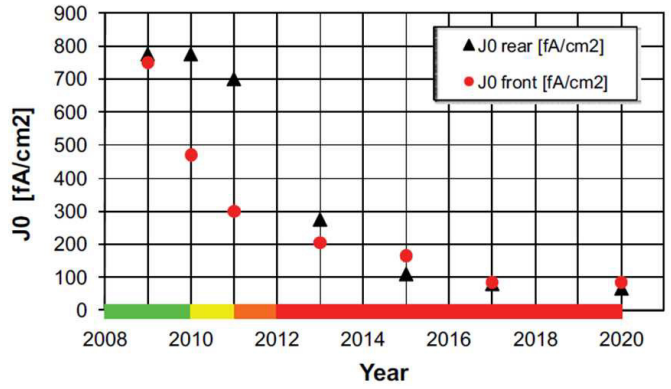

Fig. 5. Front saturation currents (emitter saturation current) and rear saturation current development [2].

be passivated with novel dielectrics that enhance the optical properties of the anti-reflection coating.

2.2 Anti-reflection coating (ARC)

Furthermore, PECVD SiN is one of the most expensive process steps. By further increasing the production capacity as predicted the use of gases like silane will increase. In future solar cell production the circumvention of silane would be preferable. SiN produced with the silane free precursor from Sixtron Applied Materials has been applied in a solar cell production run. Local Al BSF cells has been manufactured and a best cell result of 18.6% has been achieved using the silane free SiN as an ARC. Using it in the rear side passivation stack on top of SiO_x, best cell results in local Al BSF solar cells have been measured to be 18.3% [4].

2.3 Pre-passivation cleaning

Cleaning is an underestimated process for the next-generation crystalline Si solar cells. If efficiencies >20% are to be obtained, maintaining high bulk lifetimes is required. The present cleaning sequences within photovoltaic manufacturing has not been developed for this purpose. High lifetime processing will require very efficient cleaning and handling methods in view of metal contaminants. It is obvious that there is an valuable knowledge base within the microelectronics (development of ultraclean surface processes) to be taken advantage off, although it must be realized that eventually the allowable surface contamination level at a cleaned surface will be lower for crystalline Si solar cells with efficiency potential >21% than for a typical clean in advanced CMOS-processing. For the latter a lower level metallic contamination of 10^{10} cm^{-2} is acceptable but for crystalline Si solar cells metal contamination levels of 10^9 cm^{-2} might be required [5]. This is a serious challenge in terms of cost-effectiveness of the cleaning and drying process as well as on the level of characterization of such low levels of metallic contaminants on non-mirror polished or even textured Si-surfaces.

We have improved the homogeneity of ALD-grown Al_2O_3-layers for surface passivation by an adapted cleaning and drying using a Marangoni dryer [6]. Also the reduction of interface contamination in case of a-S:H heterojunctions is key to obtain high open-circuit voltages [7]. Figure 6 depicts the influence of surface conditioning cleanings of the minority carrier lifetime. The lifetime measurements have been performed on 4-inch fz-Silicon wafer (1−3 Ω cm) using QSSPC [8].

2.4 Rear-side passivation

In the framework of the investigation for high-k dielectrics which are necessary to achieve low gate leakage currents in scaled CMOS transistors, atomic layer deposition (ALD) of Al_2O_3 has been investigated intensively in the past [9]. Although the density of interface traps at the Si-Al_2O_3-interface is low, the high negative charge present in this material is an issue for CMOS transistor because it affects the threshold voltage of the device. This on the other hand is useful for applications in photovoltaic devices where the negative charge gives rise to a highly accumulated surface in p-type substrates or highly inverted surfaces in n-type substrates. As a result very low surface recombination velocities have been measured on both n- and p-type substrates [10] as well as low emitter saturation current densities on B- and P-emitters. The advantages of Al_2O_3 layers have been demonstrated in fz-Si, small area, high-efficiency crystalline Si solar cells with efficiencies up to 23% [11].

Introducing these layers in industrial solar cell flows (large area, cz-Si, 1−3 Ω cm) efficiencies up to 19% have been reported by Gatz et al. [12] on cz-Si material (2−3 Ω cm) with a thickness of 180 um. A best cell conversion efficiency of 19.1% has been achieved in IMEC [13] on cz-Si material (1−3 Ω cm) with a thickness of 150 um.

2.5 Junction formation

Achieving enhanced cell performance requires optimal dimensional control of doping profiles. Ion implantation

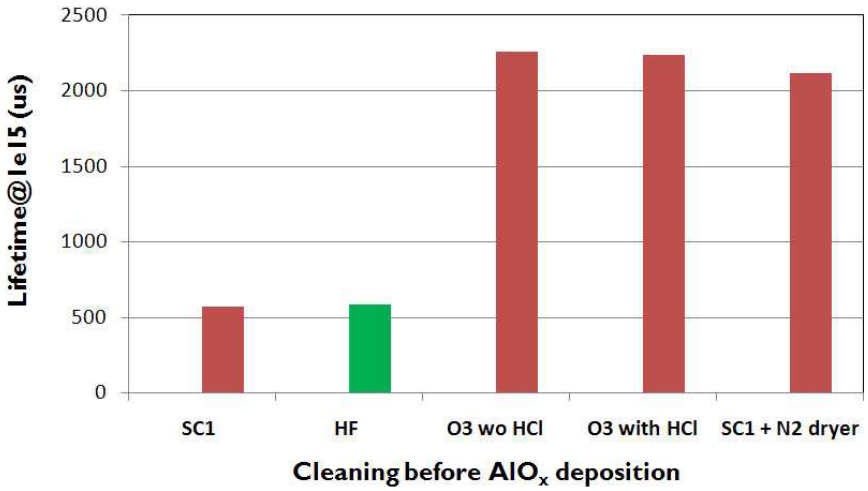

Fig. 6. Influence of surface conditioning provided by different cleanings on minority carrier lifetime. The lifetime is given in microseconds and measured at an injection level of 1e15 cm^{-3}. SC_1: NH_3:H_2O_2:H_2O mixture, HF: hydrofluoric acid, O_3 wo HCl: ozone without hydrochloric acid, O_3 with HCl: ozone with hydrochloric acid, SC_1+N_2 dryer: NH_3:H_2O_2:H_2O mixture + Nitrogen dryer.

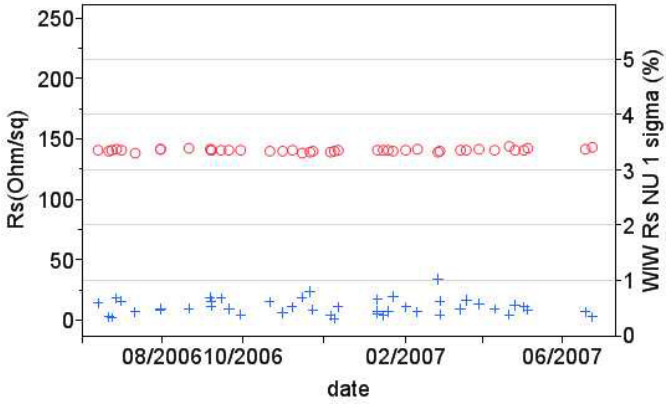

Fig. 7. Wafer to wafer reproducibility recorded over one year in a P-implantation system at IMEC aiming on 120 Ω/sq emitter.

with its excellent areal uniformity and run-to-run producibility provide a possible alternative to diffusion for shallow emitters or doping profiles difficult to achieve by diffusion processes. Wafer to wafer reproducibility, recorded over one year, for a 120 Ω/square emitter based on P-implantation was found to vary by 1.4% whereas the variation on the within wafer non uniformity was as low as 0.6% (Fig. 7). The combination with hard masks can also lead to substantial reduction in the number of steps to achieve locally doped regions in PERL and IBC cell concepts.

Emitter saturation current density (Joe) has been extracted from lifetime measurements and plotted versus corresponding emitter sheet resistance values. For sheet resistances above 100 Ω/sq, Joe below 100 fA/cm^2 has been reached using conventional PECVD SiN emitter passivation. Saturation current density values lower than 10 fA/cm^2 could be reported on 200−400 Ω/sq emitter using a stack of thermally grown silicon oxide (TO_x) and SiN as an emitter passivation dielectric layer. For advanced emitter, suited for the implementation in PERL cell concepts we have achieved an emitter saturation current density of 17 fA/cm^2 on 140 Ω/sq sheet resistance emitter with $POCl_3$ diffusion and TO_x+SiN passivation. We have achieved 55 fA/cm^2 emitter saturation current density on 132 Ω/sq sheet resistance emitter with P-implantation and thermally grown silicon oxide (TO_x) passivation (Fig. 8). The achieved results are compared with literature values of Moschner et al. [14] and Kerr et al. [15].

We have reported earlier [16] conversion efficiencies of over 18.8% for n-type emitter. Now we reached up to 19% conversion efficiency with a shallow 120 Ω/sq implanted emitter (independently confirmed by ISE Cal Lab).

2.6 Contacting

In the roadmap outlined by the SEMI-PV Group the amount of Ag/W_p is to be reduced given the weight of the Ag-cost in the total cost. In addition, this reduction or eventually fully avoiding Ag is required to ensure sustainability of crystalline Si solar production on longer term. The use of Ag would exclude production levels much higher than 100 GW_p/year [17]. Options to replace Ag are Al or Cu with the last one having the advantage of lower resistivity.

In the microelectronics sector the replacement of Al by Cu in advanced CMOS processing took place in the time period around 2000. This replacement was enabled by the use of ALD and barrier technology to avoid direct contact between the Cu contact and Si which would lead to the destruction of the junctions by the rapid indiffusion of Cu already at moderate temperatures. In CMOS technology these barriers are based on elemental metals like Ti or Ta, nitrides (TaN, ...) or silicides. Other potential issues caused by introducing copper contacts are ghost plating

Table 1. Large area cell results (cz-Si, 1−3 Ω cm) reached with AlO_x based rear-passivation dielectric layer stack. The AlO_x passivation and the SiN_x capping layers have a thickness of 10 and 110 nm, respectively.

Cell type		Size (cm^2)	Jsc (mA/cm^2)	Voc (mV)	FF (%)	Eta (%)
Al_2O_3 pass. PERC	Average (4 cells)	148.25	38.0 ± 0.2	643 ± 1	77.6 ± 0.2	19.0 ±0.1
	Best cell	148.25	38.2	645	77.7	19.1
SiO_x pass. i-PERC	Best cell	148.25	37.8	638	77.7	18.7

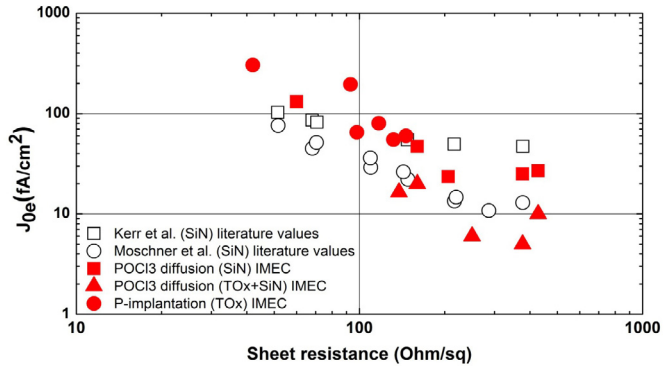

Fig. 8. Emitter saturation current density vs. emitter sheet resistance extracted from lifetime measurements. Full symbols are representing IMEC results, while hollow symbols are representing values published in literature for emitters passivated with SiN_x [14,15]. Full squares are $POCl_3$ diffused emitter passivated with PECVD SiN, Full triangles are $POCl_3$ diffused emitter passivated with a thermally grown Silicon oxide (TO_x) and SiN stack, full circles are P-implanted emitter passivated with thermal oxide. These lifetime measurements have been performed in IMEC on 1−3 Ω cm, 4-inch, fz-Silicon wafer and extracted from QSSPC measurements.

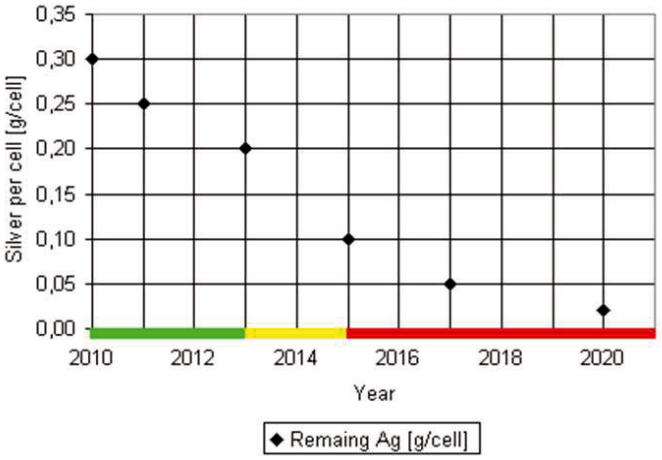

Fig. 9. Predicted development of the weight of silver in gram/cell in silicon solar cell manufacturing [2].

(diffusion through dielectric pinholes/defects during plating), reliability issues (effective barrier during subsequent processing and at operating conditions (25 years)), and corrosion (copper corrosion of the Cu capping) as shown in Figure 10. The Cu-layers in advanced circuits are normally realized by electroplating whereas the barrier layers are grown by sputtering or ALD.

We have applied different barrier layers by means of physical vapor deposition (sputtering) under Cu based contacts on the front side of the solar cell, conversion efficiencies between 19 and 19.5% were obtained on large-area solar cells using layers like Ti, Ta, TaN and $NiSi_2$. Best cell results are summarized in Table 2. By optimizing the metal grid spacing at the front side to the sheet resistance of the emitter for the 120 Ω/square case, simulations and analytic modeling have predicted for this technology efficiencies up to 20% [18].

Table 2. Overview of efficiencies obtained with various barrier layer structures on large-area crystalline Si solar cells with local Al-BSF at the rear side and Cu-based contacts at the front side. All barrier layers have been applied by physical vapor deposition (sputtering).

Contact Layer	Emitter	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	η (%)	R_s ($\Omega\,cm^2$)
Ti	60	38.4	639	79.1	19.4	5
Ti	135	38.8	651	75.6	19.1	1.1
Ta	60	38.2	640	77.9	19.0	0.82
TaN	60	38.3	636	77.8	19.0	0.78
T1/7iN	60	38.1	638	77.7	18.9	0.76
Ni	60	38.3	639	77.7	19.0	0.69

3 Conclusions

The photovoltaic sector is confronted with the challenge to reduce cost whilst at the same time increasing efficiency to reach grid parity as soon as possible and to be on equal footing with other sources of renewable energy like wind energy. For crystalline Si solar cells the gap between the theoretical limit of 30% (auger limit) and the manufactured cell efficiency of 17.5% for mono-crystalline material has to be bridged. To do so, there is still plenty of room to absorb and adapt technologies up till now limited to micro-electronics. Several examples were given, showing that this is indeed occurring at the moment for techniques like implantation, atomic layer deposition, Cu-plating and barrier layer technology with the obvious requirement that costs should be brought down to make it compatible with PV cost requirements. The interaction between the 2 sectors might not be limited to taking over elements from the technology toolbox but might also extend to the more operational issues dealing with statistical process control,

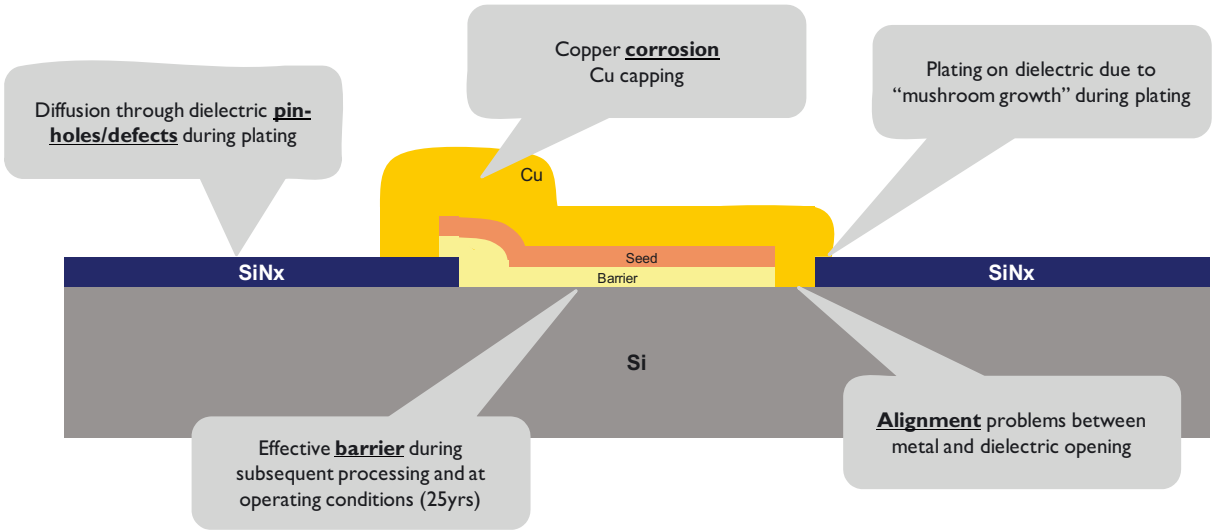

Fig. 10. Issues related to Cu-metallization (schematic).

Table 3. Best cell efficiencies achieved with the semiconductor toolbox technology implemented into an i-PERL process flow (large area cells, cz-Si, 1−3 Ω cm).

Toolbox process implemented in i-PERL cell (cz-Si, 1−3 Ω cm, 150 um thick, 148 cm^2)	Best cell efficiency [%]
Silane free SiCN as ARC	18.6
Implanted n+ Emitter	18.9
AlO_x/SiN_x rear passivation stack	19.1
Cu plated front contact	19.4

quality insurance and in-line analysis. A crucial role is given to the system suppliers, their willingness to adapt to the requirements of photovoltaic processes will at the end decide over the possible implementation of a developed technology in a silicon solar cell manufacturing line.

We have developed a semiconductor process toolbox for further decreasing the opto-electrical losses in industrial large area crystalline silicon solar cells. The developed processes are finally integrated into an industrial PERL cell concept that acts as technology demonstrator. The process integration has been performed on large area 148 cm^2, 1−3 Ω/cm resistivity, cz-silicon substrates with a thickness of 150 um. The successful implementation of the following processes in local Al BSF cells has been demonstrated and is depicted in Table 3 (best cell efficiency).

References

1. W. Sinke, C. del Cañizo, G. del Coso Sánchez, 1 € per watt-peak advanced crystalline silicon modules: the crystalclear integrated project, *Proceedings of the 23rd EU PVSEC – PV Conf* (Valencia, 2008)
2. International Technology Roadmap for Photovoltaics (ITRPV.net) Results, http://www.itrpv.net/doc/roadmap_itrpv_2011_brochure_web.pdf
3. D.H. MacDonalds, Ph.D. thesis, ANU, Australia, 2001
4. V. Prajapati, J. John, J. Poortmans, R. Mertens, Silane free high-efficiency industrial silicon solar cells using dielectric passivation and local BSF, *Proceedings of the 25th EU PVSEC – PV conf.* (Valencia, 2010)
5. A. Istranov, T. Buonassisi, M. Picketta, M. Heuer, E. Weber, Mater Sci. Eng. B **134**, 282 (2006)
6. M.M. Heyns, T. Bearda, I. Cornelissen, S. DeGendt, R. Degraeve, G. Groeseneken, C. Kenens, D.M. Knotter, L.M. Loewenstein, P.W. Mertens, S. Mertens, M. Meuris, T. Nigam, M. Schaekers, I. Teerlinck, W. Vandervorst, R. Vos, K. Wolke, IBM J. Res. Devel. **34** (1999)
7. D.A. Buchanan, E.P. Gusev, E. Cartier, H. Okorn-Schmidt, K. Rim, M.A. Gribelyuk, A. Mocuta, A. Ajmera, M. Copel, S. Guha, N. Bojarczuk, A. Callegari, C. D'Emic, P. Kozlowski, K. Chan, R.J. Fleming, P.C. Jamison, I. Brown, R. Arndt, 80 nm poly-silicon gated n-FETs with ultra-thin AI203 gate dielectric for ULSI applications, *IEDM Proceedings* (2000), pp. 223–226
8. R. Sinton, A. Cuevas, Appl. Phys. Lett. **69**, 2510 (1996)
9. G. Agostinelli, A. Delabie, P. Vitanov, Z. Alexieva, H. Dekkers, S. De Wolf, G. Beaucarne, *Solar Energy Mater. Solar Cells* **90**, 3438 (2006)
10. A. Richter, S. Henneck, J. Benick, M. Hörteis, M. Hermle, S.W. Glunz, Firing Stable Al_2O_3/SiN_x Layer Stack Passivation for the Front Side Boron Emitter of n-type Silicon Solar Cells, *Proceedings of the 25th European Photovoltaic Solar Energy Conference and Exhibition*, Valencia, pp. 1453−1456
11. J. Benick, N. Bateman, M. Hermle, Very Low Emitter Saturation Current Densities on Ion Implanted Boron Emitters, *Proceedings of the 25th European Photovoltaic Solar Energy Conference and Exhibition*, Valencia, pp. 1169–1173
12. S. Gatz, H. Hannebauer, R. Hesse, F. Werner, A. Schmidt, T. Dullweber, J. Schmidt, K. Bothe, R. Brendel, Phys. Status Solidi RRL **5**, 147 (2011)
13. B. Vermang, H. Goverde, A. Lorenz, A. Uruena, G. Vereecke, J. Das, J. Meersschaut, P. Choulat, E. Cornagliotti, A. Rothschild, J. John, J. Poortmans, R. Mertens. On the blistering of

Al2O3 passivation layers for p-type Si PERC, *Proceedings of the 26th European Photovoltaic Solar Energy Conference and Exhibition* (Hamburg, 2011)

14. J. Moschner, J. Henze, J. Schmidt, R. Hezel, *Prog. Photovolt. Res. Appl.* **12**, 21 (2004)
15. M. Kerr, J. Schmidt, A. Cuevas, J. Bultman, J. Appl. Phys. **89**, 71
16. T. Janssens, N.E. Posthuma, B.J. Pawlak, E. Rosseel, J. Poortmans, Implantation for an Excellent Definition of Doping Profiles in Si Solar Cells, *Proceedings of the 25th European Photovoltaic Solar Energy Conference and Exhibition* (Valencia, 2010), pp. 1179−1181
17. A. Feltrin, A. Freundlich, Renew. Energy **33**, 180 (2008)
18. K. Van Wichelen, L. Tous, A. Tiefenauer, C. Allebé, T. Janssens, P. Choulat, J.L. Hernàndez, E. Cornagliotti, M. Debucquoy, A. Ruocco, J. John, P. Verlinden, F. Dross, K. Baert, Towards 20.5% efficiency PERC Cells by improved understanding through simulation, published in *Proceedings of Silicon PV 2011 (Energy Procedia)* (Freiburg, Germany, 2011)